PHILIPS

50 MHz Digital Storage Oscilloscope
PM3335 – PM3337

TEST & MEASUREMENT *CUSTOMER SUPPORT*

4822 872 05332
890401/1

Service Manual

Service Supplement

CUSTOMER SUPPORT

SSU05345-2

950303
4822 872 09444

Related to: **PM3335/37** SERVICE MANUAL 4822 872 05345

Already published for this manual: SSU05345-1

Subject/purpose/symptom: **CLASS 4**
1 - Information on how to use the PM3335/37 Service Manual for PM3331
2 - Information on RS232C + IEEE interfaces (PM8959, PM8961)

1. PM3331 - 40 MHz COMBISCOPE

GENERAL.
This information sheet deals with the differences between PM3331 and PM3335/37. The CombiScope PM3331 is derived from the model number PM3335. The bandwidth of vertical channels and triggering in PM3331 is lower than in PM3335/37. However you can use the PM3335/37 Service Manual 4822 872 05345 for repair and maintenance of PM3331. The differences are listed below.
PM3331 and PM3335/PM3337 make use of the same set of Users Manuals.

CHARACTERISTICS.
Characteristics in chapter 2 should be changed as follows for PM3331:
- Vertical bandwidth between 20 mV ... 10 V/div is 40 MHz; the belonging rise time is 8.75 ns.
- Dynamic range and cross talk between channels are specified at 40 MHz (instead of 50 MHz).
- The trigger sensitivity of >1 div (external >150 mV) ranges up to 40 MHz.
- The trigger sensitivity of >3 div (external >500 mV) ranges up to 60 MHz.

PM3335 SERVICE MANUAL CHANGES FOR USE WITH PM3331:
- Partslist changes:
  * Page 18-7: Trimming capacitor C3005 (20 pF) has been removed from XYZ unit A2.
  * Page 18-1: The PM3331 text strip (item 6) above the CRT has ordering code 5322 466 30445.
  * Page 18-17: The Eprom D9013 on unit A9 has ordering code 5322 209 52399. The D9013 Eprom for PM3335/3337 has ordering code 5322 209 51682. Eprom D102 on hardcopy interface: 5322 209 51656 (same for PM3335/PM3337).
- Performance test changes:
  * Page 13-5, 13.3.4, Auto set: use a 40 MHz sine wave instead of 50 MHz.
  * Page 13-9, 13.3.9, Frequency response: increase the frequency up to 40 MHz instead of 60 MHz.
  * Page 13-10, 13.3.10, Rise time: measured value is 8.8 ns instead of 5.8 ns (1.8 div instead of 1.16 div).

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* Page 13-14, 13.3.15, Cross talk: use a 40 MHz sinewave instead of 60 MHz.
* Page 13-28, 13.3.30, Trigger sensitivity A/B: use 40 MHz instead of 50 MHz, use 60 MHz instead of 100 MHz.
* Page 13-29, 13.3.31, Trigger sensitivity EXT: use 40 MHz instead of 50 MHz, use 60 MHz instead of 100 MHz.

- Adjusting procedure change: the C3005 adjustment step on the pages 15-8 and 15-15 can be skipped.

2. RS232C + IEEE INTERFACES

INTERFACE CONFIGURATIONS

The circuit diagram (figure 1) and the p.c.b. lay-out (figure 2) are valid for the interface configuration with full featured bidirectional RS232C + IEEE interfaces. On the same p.c.b. two less extensive interface versions are possible. This is realized by leaving out components:

- a full featured bidirectional RS232C-only interface is realized by leaving out the IC's D109, D111, D112, D113, D114.
- a RS232C screen dump interface is realized by leaving out the IC's D108, D109, D111, D112, D113, D114.

The firmware for these 3 configurations is universal. The firmware is also universal for the models PM3331, PM3335, PM3337. Firmware is present in Eprom D102.

CIRCUIT DESCRIPTION

The interface unit incorporates a microcomputer system, a RS232C interface, an IEEE interface and some control circuitry. The microprocessor system consists of processor D101 and belonging Eprom D102 and Random Access Memory D103. The RS232C interface consists of interface chip D107 with 3 input buffers D117 for the signals DSR (Data Set Ready), CTS (Clear To Send) and RXD (Receive Data). D117 converts the RS232C input levels of ±12 volt to TTL. There are also 3 output buffers D118 for the signals TXD (Transmit Data), DTR (Data Terminal Ready) and RTS (Request To Send). D118 converts TTL into RS232C levels.

The IEEE interface consists of interface IC D108 and the associated input/output buffers D111, D112, D113, D114. D108 is also present on the bidirectional RS232C-only interface; part of the communication protocol is realized in D108.

The crystal G101 provides timing both for the microcomputer and the RS232C chip. Communication between the oscilloscope's main microcomputer and the interface unit happens via the buffers D104 (bidirectional) and D106. Bufer D104 transfers data under influence of the control signals ENIEBULT (Enable IEEE Buffer) and OPTRD (Option Read). Buffer D106 transfers address information under control of the signals ENIEBULT and ALE---HT (Address Latch Enable). The PLS chip D116 makes the in and output signals that control the interface unit. The PLS is a combinatoric device where a certain input combination results in a factory-programmed output code. The input/output signals of this device are:

- Input signal X1/CLK is inverted to output signal UPCLK.
- Input signal BG----LT (Bus Grant) makes the bus free for the oscilloscope's main microcomputer system.
- Input signals A18, A19 (Address lines A18 and A19): these lines select via the D116 outputs the 4 devices that are present on this unit. They are: Eprom D102 (via ROMSL-LT/ROMselect), the RAM D103 (via CSIERALT/chipselect and WRIERALT/write), the RS232C device D107 (via CS232-LT/chip select and IEWR--LT/write), the IEEE device D108 (via CSIE--LT/chip select, RDIE--LT/read, WRIE--LT/write)

PARTS LISTS

Capacitors:

C101	4.7pF ±0.25pF	5322 122 33082
C102	4.7pF ±0.25pF	5322 122 33082
C103	33uF ±20%	5322 124 21957
C104	22nF -20/+80%	4822 122 30103
C106	22nF -20/+80%	4822 122 30103
C107	22nF -20/+80%	4822 122 30103
C108	22nF -20/+80%	4822 122 30103
C109	15uF ±20%	5322 124 21958
C111	15uF ±20%	5322 124 21958
C112	1nF ±10%	4822 122 30027
C114	1nF ±10%	4822 122 30027
C116	1nF ±10%	4822 122 30027
C118	330pF ±2%	4822 122 31353
C119	330pF ±2%	4822 122 31353
C122	330pF ±2%	4822 122 31353

Resistors:

R101	100k 1% MRS25	4822 116 52973
R102	10k array	5322 111 90473
R103, R106	3.16k 1% MRS25	4822 116 53021
R104, R107	10k 1% MRS25	4822 116 53022

Semi-Conductors:

V101, V102	BC548C	4822 130 44196
V103, V104	BAW62	4822 130 30613

Integrated Circuits:

D101	MC68008P8	5322 209 11593
D102	EPROM V4.2	5322 209 51656
D103	M62256LP-12	5322 209 72129
D104	PC74HCT245P	5322 209 11117
D106	PC74HCT573P	5322 209 11488
D107	N68681C1N40	5322 209 11561
D108	P8291A	5322 209 81264
D109	PC74HCT02P	5322 209 11106
D111, D112	MC3448AP	5322 209 11317
D113, D114	MC3448AP	5322 209 11317
D116	PLS153AN	5322 209 60478
D117	MC1489AL	5322 209 86103
D118	MC1488L	5322 209 84307

Miscellaneous:

Interface unit universal (*)	5322 214 90325
IEEE connector at rear of oscilloscope	5322 267 60258
IEEE connector (26p), fits into X102	5322 267 70175
X102 connector on p.c.b.	5322 265 40557
RS232 connector at rear of oscilloscope	5322 290 40382
RS232 connector (10p), fits into X103	5322 268 40234
X103 connector on p.c.b.	5322 265 30443
48 pole IC-socket (for D101)	5322 255 40831
32 pole IC-socket (for D102)	5322 255 40829
X150 connector on p.c.b.	5322 265 61072
Crystal G101	5322 242 71867

(*): this universal unit may incorporate more components than the one to be replaced.

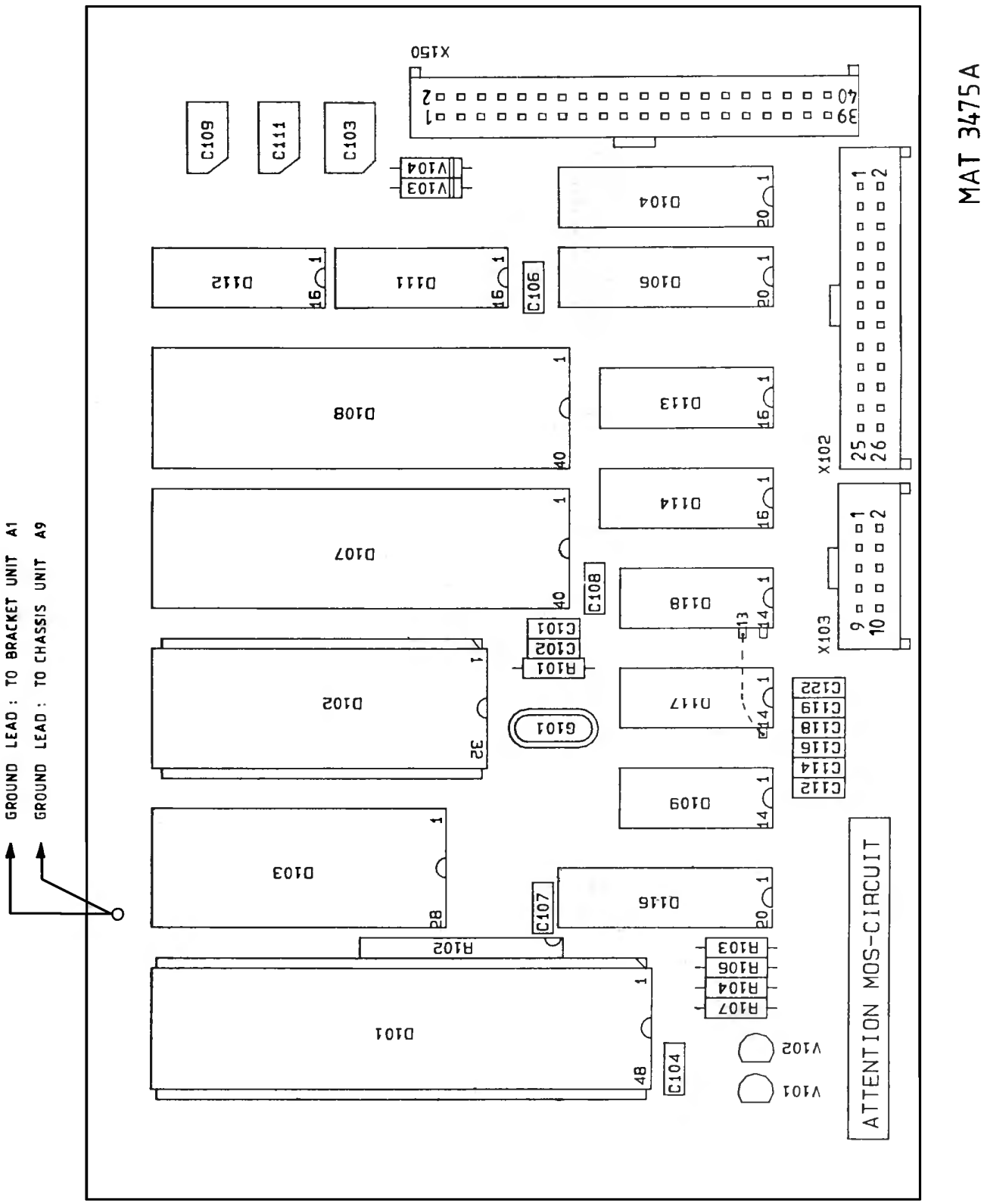
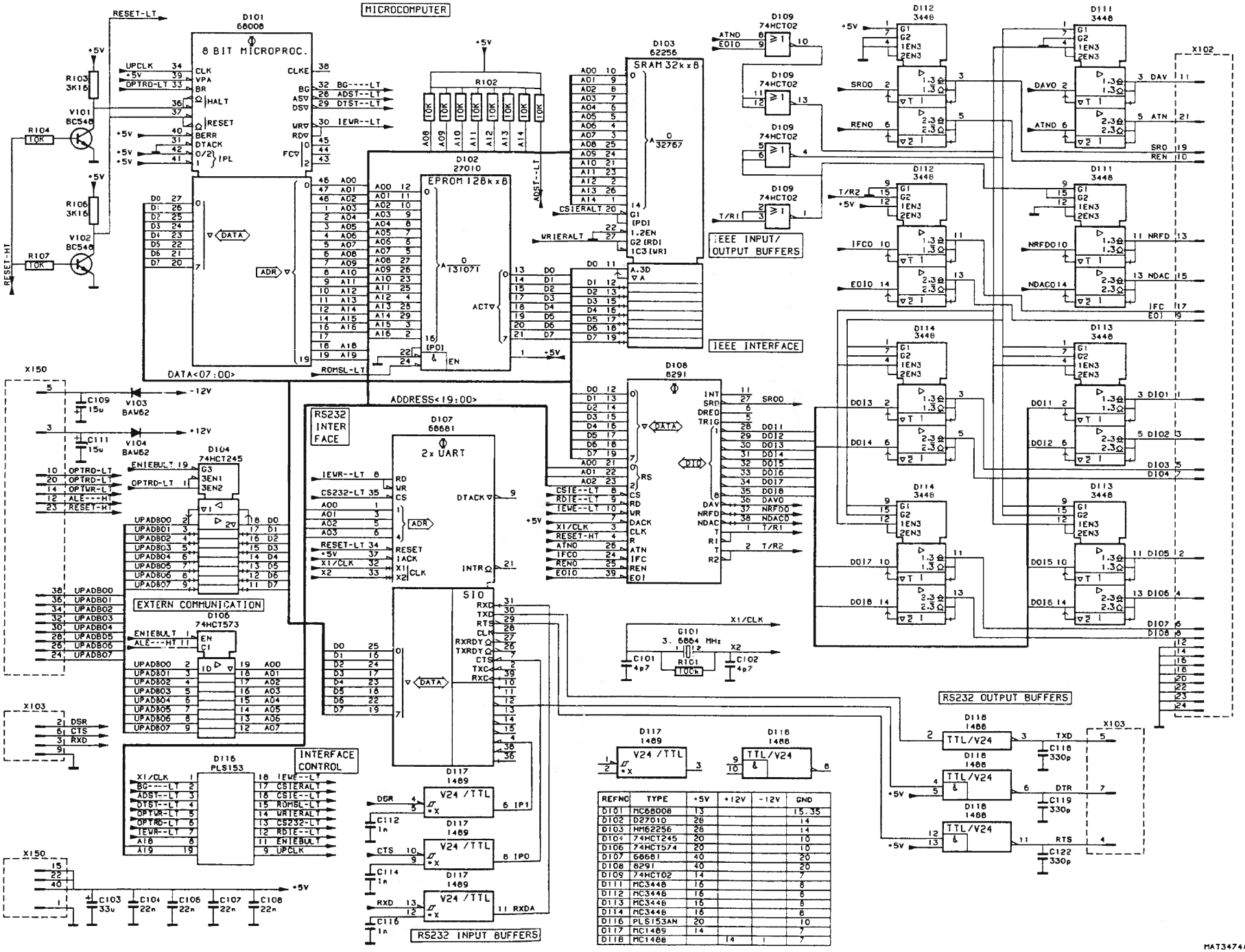


Figure 1. Printed circuit board lay-out (IEEE + RS232C configuration, see text).



REFNO	TYPE	+5V	+12V	-12V	GND
D101	MC68008	13			15,35
D102	D27010	28			14
D103	HM62256	28			14
D104	74HCT245	20			10
D106	74HCT574	20			10
D107	68681	40			20
D108	8291	40			20
D109	74HCT02	14			7
D111	MC3448	16			8
D112	MC3448	16			8
D113	MC3448	16			8
D114	MC3448	16			8
D116	PLS153AN	20			10
D117	MC1489	14			7
D118	MC1488		14	1	7

Figure 2. Circuit diagram of interface unit (IEEE + RS232C configuration, see text).

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WARNING: These servicing instructions are for use by qualified personnel only. To reduce the risk of electric shock do not perform any servicing other then that specified in the Operating Instructions unless you are fully qualified to do so.

PHILIPS

IMPORTANT: In correspondence concerning this instrument, please quote the type number and serial number as given on the type plate.

NOTE: The design of this instrument is subject to continuous development and inprovement. Consequently, this instrument may incorporate minor changes in detail from the information contained in this manual.

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CONTENTS Page

1. SAFETY INSTRUCTIONS

Read these pages carefully before installation and use of the instrument.

1.1 INTRODUCTION

The following clauses contain information, cautions and warnings which must be followed to ensure safe operation and to retain the instrument in a safe condition.
Adjustment, maintenance and repair of the instrument shall be carried out only by qualified personnel.

1.2 SAFETY PRECAUTIONS

For the correct and safe use of this instrument it is essential that both operating and servicing personnel follow generally-accepted safety procedures in addition to the safety precautions specified in this manual.
Specific warning and caution statements, where they apply, will be found throughout the manual.
Where necessary, the warning and caution statements and/or symbols are marked on the apparatus.

1.3 CAUTION AND WARNING STATEMENTS

CAUTION: is used to indicate correct operating or maintentance procedures in order to prevent damage to or destruction of the equipment or other property.

WARNING: calls attention to a potential danger that requires correct procedures or pracites in order to prevent personal injury.

1.4 SYMBOLS

High voltage $\geq$ 1000 V (red)

Live part (black/yellow)

Read the operating instructions

Protective earth (grounding) terminal (black)

1.5 IMPAIRED SAFETY-PROTECTION

Whenever it is likely that safety-protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation. The matter should then be referred to qualified technicians.
Safety protection is likely to be impaired if, for example, the instrument fails to perform the intended measurements or shows visible damage.

1.6 GENERAL CLAUSES

1.6.1 WARNING: The opening of covers or removal of parts, except those to which access can be gained by hand, is likely to expose live parts and accessible terminals which can be dangerous to live.

1.6.2 The instrument shall be disconnected from all voltage sources before it is opened.

1.6.3 Bear in mind that capacitors inside the instrument can hold their charge even if the instrument has been separated from all voltage sources.

1.6.4 WARNING: Any interruption of the protective earth conductor inside or outside the instrument, or disconnection of the protective earth terminal, is likely to make the instrument dangerous. Intentional interruption is prohibited.

1.6.5 Components which are important for the safety of the instrument may only be renewed by components obtained through your local Philips organisation. (See also section 15).

1.6.6 After repair and maintenance in the primary circuit, safety inspection and tests, as mentioned in section 15 have to be performed.

2. CHARACTERISTICS

A. Performance Characteristics

- Properties expressed in numerical values with stated tolerance are guaranteed by PHILIPS. Specified non-tolerance numerical values indicate those that could be nominally expected from the mean of a range of identical instruments.
- This specification is valid after the instrument has warmed up for 30 minutes (reference temperature 23°C).
- For definitions of terms, reference is made to IEC Publication 351-1.

B. Safety Characteristics

- This apparatus has been designed and tested in accordance with Safety Class I requirements of IEC Publication 348, Safety requirements for Electronic Measuring Apparatus, UL 1244 and CSA 556B and has been supplied in a safe condition.

C. Initial Characteristics

. Overall dimensions:

- Width

Including handle	: 387 mm
Excluding handle	: 350 mm

- Length

Including handle	: 518,5 mm
Excluding handle, excl. knobs	: 443,5 mm
Excluding handle, incl. knobs	: 455,5 mm

- Height

Including feet	: 146,5 mm
Excluding feet	: 134,5 mm
Excl. under-cabinet	: 132,5 mm

Figure 2.1 Dimensions of oscilloscope PM3335.

* Mass : 8,5 kg

* Operating positions:

  a. Horizontally on bottom feet
  b. Vertically on rear feet
  c. On the carrying handle in two sloping positions.

D. CONTENTS

	CHARACTERISTICS	SPECIFICATION	ADDITIONAL INFORMATION
2.1	DISPLAY		
	* CRT		
	Type No	PHILIPS D 14-372	
	Measuring area (h x w)	80 x 100 mm	8 x 10 div. 1 div. = 10 mm 1 subdiv. (sd) = 2 mm
	* Screen type		
	Standard	GH (P 31)	Standard persistence (7 ms)
	Option	GM (P 7)	Long persistence (30 ms)
	* Total acceleration voltage	16 kV	
	* Graticule:		
	Engravings	Internal fixed	
	Division lines	1 cm	Horizontal as well as vertical
	Subdivisions	2 mm	Horizontal as well as vertical
	Dotted lines	1,5 and 6,5 cm from top	Only horizontal.
	Percentages	0%, 10%, 90%, 100%	Left side of screen
	* Orthogonality	90^{o} +/- 1^{o}	Measured in zero point.
	* Illumination	Continuously variable	By means of potentiometer.
2.2	VERTICAL DEFLECTION OR Y AXIS		
	* Auto set	Automatic setting according to input signal	
	* Deflection modes and sources	Channel A and/or B or ADDED (A+B, A_B)	Channel B can be inverted. All combinations are possible in ALTERNATE as well as in CHOP mode
	* Deflection coefficients	2 mV/div...10 V/div	In 1, 2, 5 sequence. If probe with range indicator is used, deflection coeff. is automatically calculated in display.
	* Variable gain control range	1 : >2,5	
	* Error limit	+/- 3%	Only in calibrated position.
	* Input impedance	1 M ohm +/-2%	Measured below 1 MHz
	Paralleled by	20 pF +/-2pF	Measured below 1 MHz

CHARACTERISTICS	SPECIFICATION	ADDITIONAL INFORMATION
* Max. input voltage	400 V (d.c. + a.c. peak)	
Max. test voltage (rms)	500 V	Max. duration 60 s.
* Bandwidth for 20 mV...10 V	> 50 MHz (-3dB, amb. 15..35°C)	Input 6 div. sine-wave. Deviation max. 5MHz for ambient 0 ... 50°C
* Bandwidth for 2 mV, 5 mV and 10 mV	> 35 MHz	Input 6 div. sine-wave.
* Rise-time	7 ns or less	Calculated from 0,35/f-3 dB
* Noise 20 mV...10 V	< 0,5 sd	Measured visually. Pick up on open BNC excluded.
* Lower - 3 dB point	< 10 Hz	In AC position, 6 div. sine-wave
* Dynamic range		
@ 1 MHz	+/- 12 div.	Vernier in CAL position.
@ 50 MHz	> 8 div.	Vernier in CAL position.
* Position range	> +/- 8 div.	Vernier in CAL position.
* Cross talk between channels		Both channels same attenuator setting. Input max. 8 div. sine-wave.
@ 10 MHz	1 : > 100	2, 5 and 10 V are excluded.
@ 50 MHz	1 : > 50	2, 5 and 10 V are excluded.
* Common Mode Rejection Ratio @ 1 MHz	1 : > 100	Both channels same attenuator setting, vernier adjusted for best CMRR; measured with max. 8 div. (+/- 4 div.) each channel.
* Visible signal delay	> 15 ns	Max. intensity, measured from line start to trigger point.

CHARACTERISTICS	SPECIFICATION	ADDITIONAL INFORMATION
* Base-line jump: between attenuator steps		
20 mV...10 V	< 1 sd	
Additional jump between 10 mV <---> 20 mV	< 1,5 sd	
Normal Invert jump	< 1 sd	Only channel B.
ADD jump	< 0,6 div.	When A and B are positioned in screen centre (20 mV...10 V).
Variable jump	< 1 sd	Max.jump in any two positions of the VARiable control.

2.3 HORIZONTAL DEFLECTION OR X AXIS

2.3.1 Time Base

* Time coeff.	0,5 s...50 ns	1, 2, 5 sequence (magn.off)
Error limit	+/-3 %	Measured at -4...+4 div. from screen centre.
* Horizontal position range	Start of sweep and 10th div. must be shifted over screen centre	
* Variable control ratio	1 : > 2,5	
* Time Base magnifier	Expansion x10	Not valid in X-deflection.
Error limit	+/-4 %	Measured at +4...- 4 div. from screen centre. Excluding first 50 ns and last 50 ns.
* Horizontal magnifier balance x10 ---> x1	< 2,5 sd	Shift start of sweep in x10 in mid-screen position, then switch to x1.
* Hold-Off Minimum to maximum hold-off time ratio	1 : > 10	Minimum hold off time is related to time base setting.

	CHARACTERISTICS	SPECIFICATION	ADDITIONAL INFORMATION
2.3.2	X-deflection		
	* Deflection coeff. Via channel A or B	2 mV/div...10 V/div	1, 2, 5 sequence.
	Via EXT input	100 mV/div.	
	* Error limit Via channel A or B	+/- 5%	
	Via EXT input	+/- 5%	
	* Bandwidth	DC .... > 2 MHz	DC coupled
	* Phase shift between X and Y-deflection	$< 3^{o}$ @ 100 kHz	DC coupled
	* Dynamic range	> 24 div. DC... 100 kHz	DC coupled
2.3.3	EXT input		
	* Input impedance	1 M ohm +/- 2%	f_o < 1 MHz
	Paralleled by	20 pF +/- 2 pF	f_o < 1 MHz
⚠	* Max. input voltage	400 V (d.c. + a.c. peak)	
	Max. test voltage (rms)	500 V	Max. duration 60 s.
	* Lower - 3 dB point	< 10 Hz	AC coupled
2.4	TRIGGERING		
	* Trig. mode AUTO (auto free run)	Bright line in absence of trigger signal	Auto free run starts 100 ms (typ.) after no trig.pulse.
	TRIGgered		Switches automatically to auto free run if one of the display channels is grounded.
	SINGLE		In multi-channel mode (alternated) each channel is armed after reset; if sweep has already started, sweep is not finished. Not applicable in peak-to-peak coupling.
	* Trigger source A, B, Composite (A/B), EXT, Line		Line trigger source always triggers on mains frequency. Line trigger amplitude depends on line input voltage. Approx. 6 div. @ 220 VAC input voltage.

CHARACTERISTICS	SPECIFICATION	ADDITIONAL INFORMATION
* Trigger coupling Peak-to-peak (p-p), DC, TVL, TVF		
* Level range		
Peak-to-peak:	Related to peak-to-peak value	p-p coupling is DC rejected.
DC internal	> (+ or - 8 div.)	
DC EXTernal	> (+ or - 800 mV)	
TVL/TVF	Fixed level	
* Trigger slope	+/-	Slope sign in LCD. For TVL/TVF use + or - to chose positive or negative video
* Trigger sensivity		
INTERNAL		
0 - 10 MHz	< 0,5 div.	Trig. coupling DC.
@ 50 MHz	< 1,0 div.	Trig. coupling DC.
@ 100 MHz	< 3,0 div.	Trig. coupling DC.
EXTERNAL		
0 - 10 MHz	< 50 mV	Trig. coupling DC.
@ 50 MHz	< 150 mV	Trig. coupling DC.
@ 100 MHz	< 500 mV	Trig. coupling DC.
TVL/F INTERNAL	< 0,7 div.	Sync. pulse.
TVL/F EXTERNAL	< 70 mV	Sync. pulse.

2.5 SIGNAL ACQUISITION

* Sampling type @10us/div ... 50s/div	Real time	
* Maximum sample rate:		Sample rate depends on time/div setting
single channel	20 Megasamples/s	
dual channel	20 Megasamples/s	
* Vertical (voltage) Resolution	8 bits	(=0,4% of full range of 10 div)

CHARACTERISTICS	SPECIFICATION	ADDITIONAL INFORMATION
* Horizontal (time) Resolution: in single channel acquisition:		
in 20us/div... 50s/div	8192 samp./ acquisition	1 Sample = 0,0125% of full record.
10 us/div	4096 samp./ acquisition	1 Sample = 0,024% of full record.
in dual channel acquisition 10us ...50s/div	4096 samp./ acquisition	1 Sample = 0,024% of full record.
* Record length	20,4 x time/div	Display in unmagnified position.
* Acquisition time: real time 10us/div ...	20,4 x time/div	
50s/div	+ 0 ... 20ms	excluding delay time
* Sources	Channel A Channel B	Channel B can be inverted before acquisition.
* Acquisition modes	1 Channel only	Full memory available for 1 channel.
	2 Channels	Simultaneously sampled; 2 channels share memory.

2.6 CHANNELS A AND B

* Frequency response: Lower transition point of BW		
Input coupling in DC position	d.c.	
Input coupling in AC position	$\leq$ 10Hz	
Upper transition point of BW:		
In memory on mode (Ambient: 15 ... 35 °C)	$\geq$ 10MHz(-3dB)	Deviation max. 3MHz for ambient: 0 ... 50 °C.
In memory off mode (Ambient: 15 ... 35 °C)	$\geq$ 50MHz(-3dB)	Deviation max. 5MHz for ambient: 0 ... 50°C.

CHARACTERISTICS	SPECIFICATION	ADDITIONAL INFORMATION
* Max. base line instability: Jump (Ambient: 15 ... 35 °C):		Add 25% for ambient: 0 ... 50 °C.
when switching to memory mode:	0,3 div	
when actuating INVertor switch between any time /div positions	0,3 div 0,5 div	
Drift	0,1 div/h	}Measured in 20 mV/div
Temperature coefficient	± 0,05 div/K	}position. }

2.7 TIME BASE

* Modes	Recurrent Single shot Multiple shot	Up to 2 shots.
* Time coefficients: in recurrent	10 us/div ... 50 s/div	
in single shot & multiple shot	10 us/div ... 50 s/div	
error limit (Ambient 15 .. 35°C) in real time mode	±1%	Add 0,5% for ambient: 0 ... 50 °C.
up to memory	±0,1%	

2.8 TRIGGER

* Trigger delay: range	-20 ... 0 div	Selectable in divisions.
accuracy	± 0,3 div	
* Trigger level view		Indication in LCD.
inaccuracy	≤ 0,5 div	

	CHARACTERISTICS	SPECIFICATION	ADDITIONAL INFORMATION
2.9	MEMORY		
	* Memory size:		
	registers	2	
	register depth:		
	acquisition	8K words	
	register	8K words	
	wordlength	8 bits	
	* Functions	Clear	
		Load	Contents of acquisition are saved in register
		Lock	Memory system is locked. If lock is not active the signal is written into the acquisition memory.
2.10	DISPLAY		
	* Sources	Channel A	}
		Channel B	}In any combination
		Register A	}
		Register B	}
	* Display expansion horizontal	0,5x, 1x, 2x, 4x, 8x, 16x and 32x.	
	* Number of displayed samples:		
	single trace	4K/channel	
	two traces	2K/channel	
	three traces	1K/channel	
	four traces	1K/channel	
2.11	CALCULATION FACILITIES		
	* Functions	Ratio, Phase	
		dV, dt, 1/dt	
2.12	AUTO SETTING		
	* Settling time	3s (typ.)	Auto set is done in analog mode.

	CHARACTERISTICS	SPECIFICATION	ADDITIONAL INFORMATION
2.13	CURSORS		
	* Horizontal resolution: in single channel mode	1:1000	Over 10 div
	in dual channel mode	1:1000	
	* Vertical resolution	1:200	8 div
	* Read out resolution	3 Digits	
	* Voltage cursors: error limit amb. 15 ... 35 °C	±3%	Referred to input at BNC, error of probes etc. excluded. Add 3% for ambient 0 .. 40 C.
	cursor range	Full range	Cursors can not pass not each other. X-position is neglected.
	* Time cursors error limit	±0,1%	
2.14	POWER SUPPLY		
⚠	* Line voltage a.c.		One range.
	Nominal	100...240 V	
	Limits of operation	90...250 V	
	* Line frequency		
	Nominal	50...400 Hz	
	Limits of operation	43...445 Hz	
	* Safety requirements within specification of: IEC 348 CLASS I UL 1244 VDE 0411 CSA 556 B		
	* Power consumption (a.c. source)	55W nominal	At nominal source voltage

	CHARACTERISTICS	SPECIFICATION	ADDITIONAL INFORMATION
2.15	SUNDRIES		
	* Z-MODulation		TTL-compatible.
	ViH	> 2,0 V	Blanks display.
	ViL	< 0,8 V	Max. intensity Analog control between ViH and ViL is possible.
	* CAL output		To calibrate drop or tilt of probes.
	Output voltage	1,2 V +/- 1%	Rectangular output pulse.
	Frequency	2 kHz	
	The output may be short-circuited to ground.		
	* Data and settings retention:		When instrument is switched off or during mains faillure. The oscillooscope settings and traces are saved before instrument goes down.
	memory back-up voltage	2V ... 3,5V	
	memory back-up current drain	Typical 100uA	@25 °C.
	recommended batteries:		According to IEC285 (=Alkaline Manganese Penlight Battery)
	type	LR 6	e.g. PHILIPS LR 6.
	quantity	2 pcs	Delivered with the instrument.
	temperature rise of batteries	20K	After warming up period of instrument.
	retention time	typical 3 years	@ 25°C, with recommended (fresh) batteries.
	* Temperature range	0 ... +70°C.	@ -40 ... 0 °C settings retention is uncertain. It is advised to remove batteries from instrument when it is stored during longer (24h) period below -30°C or above 60°C. WARNING: UNDER NO CIRCUMSTANCES BATTERIES SHOULD BE LEFT IN INSTRUMENT @ TEMPERATURES BEYOND THE RATED RANGE OF THE BATTERY SPECIFICATIONS!

CHARACTERISTICS	SPECIFICATION	ADDITIONAL INFORMATION

2.16 ENVIRONMENTAL CHARACTERISTICS

The environmental data mentioned in this manual are based on the results of the manufacturer's checking procedures.
Details on these procedures and failure criteria are supplied on request by the PHILIPS/FLUKE organisation in your country, or by PHILIPS, INDUSTRIAL AND ELECTRO-ACOUSTIC SYSTEMS DIVISION, EINDHOVEN, THE NETHERLANDS.

* Meets environmental requirements of:	MIL-T-28800 C, type III, CLASS 5 Style D	Class 5, except for operating temperature: 0 ... 40 °C. Style D, except for front cover.
* Temperature:		Memory back-up batteries removed from instrument, unless batteries meet temperature specifications (see also 2.15).
operating:		
min. low temperature	0 °C	Cf. MIL-T-28800 C parr. 3.9.2.3. tested cf. par. 4.5.5.1.1.
max. high temperature	+50 °C	Cf. MIL-T-28800 C parr. 3.9.2.4. tested cf. par. 4.5.5.1.1.
non-operating (storage):		
min. low temperature	-40 °C	Cf. MIL-T-28800 C parr. 3.9.2.3. tested cf. par. 4.5.5.1.1.
max. high temperature	+75°C	Cf. MIL-T-28800 C parr. 3.9.2.4. tested cf. par. 4.5.5.1.1.
* Max. humidity operating non-operating	95% RH	+10...30°C
* Max. altitude:		MIL-T-28800 C par. 3.9.3. tested, par. 4.5.5.2.
operating	4,5 km (15000 feet)	Maximum. Operating Temperature derated 3°C for each km, for each 3000 feet, above sea level.
non-operating (storage)	12 km (40 000 feet)	

CHARACTERISTICS	SPECIFICATION	ADDITIONAL INFORMATION
* Vibration (operating)		MIL-T-28800 C par. 3.9.4.1. tested, par. 4.5.5.3.1.
Freq. 5...15 Hz		
Sweep Time	7 min.	
Excursion (p-p)	1,5 mm	
Max Acceleration	7 m/s^2 (0,7 x g)	@ 15 Hz
Freq. 15...25 Hz		
Sweep Time	3 min.	
Excursion (p-p)	1 mm	
Max Acceleration	13 m/s^2 (1,3 x g)	@ 25 Hz
Freq. 25...55 Hz		
Sweep Time	5 min.	
Excursion (p-p)	0,5 mm	
Max Acceleration	30 m/s^2 (3 x g)	@ 55 Hz
Resonance Dwell	10 min.	@ each resonance freq. (or @ 33 Hz if no resonance was found). Excursion, 9.7.1. to 9.7.2.
* Shock (operating)		MIL-T-28800 C par. 3.9.5.1. tested, par. 4.5.5.4.1.
Amount of shocks		
total	18	
each axis	6	3 in each direction.
Shock Wave-form	Half sine-wave	
Duration	11 ms	
Peak Acceleration	300 m/s^2 (30 x g)	
* Bench handling		MIL-T-28800 C par. 3.9.5.3. tested cf. par. 4.5.5.4.3.
Meets requirements of	MIL-STD-810 method 516, proced. V	
* Salt Atmosphere		MIL-T-28800 C par. 3.9.8.1 tested, par. 4.5.6.2.1.
Structural parts meet requirements of	MIL-STD-810 method 509, proced. I salt solution 20%	
* EMI (Electronic Magnetic Interference)		
meets requirements of	MIL-STD-461 CLASS B	Applicable requirements of part 7 : CE03, CS01, CS02, CS06, RE02, RS03
	VDE 0871 and VDE 0875 Grenzwertklasse B	

	CHARACTERISTICS	SPECIFICATION	ADDITIONAL INFORMATION
2.17	SAFETY		
	* Meets requirements of	IEC 348 CLASS I VDE 0411	Except for power cord, unless shipped with Universal European power plug.
		UL 1244 CSA 556 B	Except for power cord, unless shipped with North American power plug.
2.18	OPTIONAL VERSIONS		
	* General		These options can be factory installed only.
	* Power cord		Length 2,1 m (82,7 in)
		Universal European	VDE, KEMA listed (option .01)
		North American	CSA, UL listed (option .03)
		United Kingdom	BSI listed (option .04)
		Australian	SAA listed (option .08)
		Swiss	SAV listed (option .05)
	* Cabinet	Rack mount	PM3337 PM3337/40. with IEEE+RS232-interface installed.
	* Interface	IEEE-488/IEC-625 including RS 232-C	Option 40. Dump to plotters: PM 8153/1, PM 8153/6, PM 8154, PM 8155, HP 7475A and HP 7550. Dump to printers: FX80 and HP 2225 Thinkjet.
		RS 232-C dump only	Option 50. Dump to plotters: PM 8153/1, PM8153/6, PM 8154, PM 8155, HP 7475A and HP 7550. Dump to printers: FX80 and HP 2225 Thinkjet.

3. INTRODUCTION TO CIRCUIT DESCRIPTION AND BLOCK DIAGRAM DESCRIPTION

3.1 INTRODUCTION TO CIRCUIT DESCRIPTION

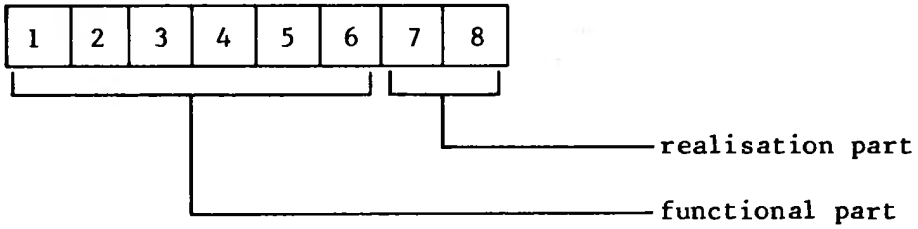
3.1.1 General

The functioning of the circuits is described per printed-circuit board (p.c.b.). For every p.c.b. (unit) a separate chapter is available containing the lay out of the p.c.b., the associated circuit diagram(s) the circuit description and a signal name list.

3.1.2 Explanation of signal name set-up

Signal name consists of two parts:

- a functional part of maximal 6 characters
- a realisation part of 2 characters



The realisation part is optional. If it is used then the functional parts should consist of 6 characters. If necessary dummies (minus sign) are used in the functional part, to make it 6 characters long.

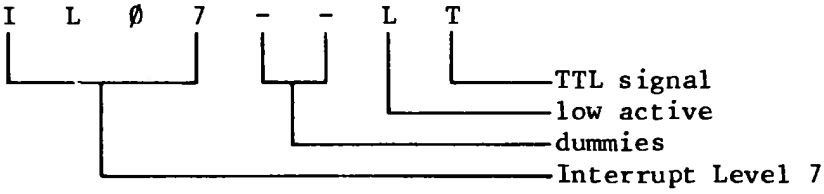
The first character of the realisation part has the following meaning:

H: active high signal
L: active low signal
X: irrelevant (e.g. counter outputs)

The second character of the realisation part is used to identify signal levels:

A: analogue
C: CMOS 12 V or 15 V
D: CMOS 5 V
E: ECL -4,5 V or -5,2 V
T: TTL 5 V or HCT

Example: I L Ø 7 - - L T



Sometimes the functional part can also be used for a serial number e.g. to indicate a buffered version of a signal.

Example: CHPT--Ø1

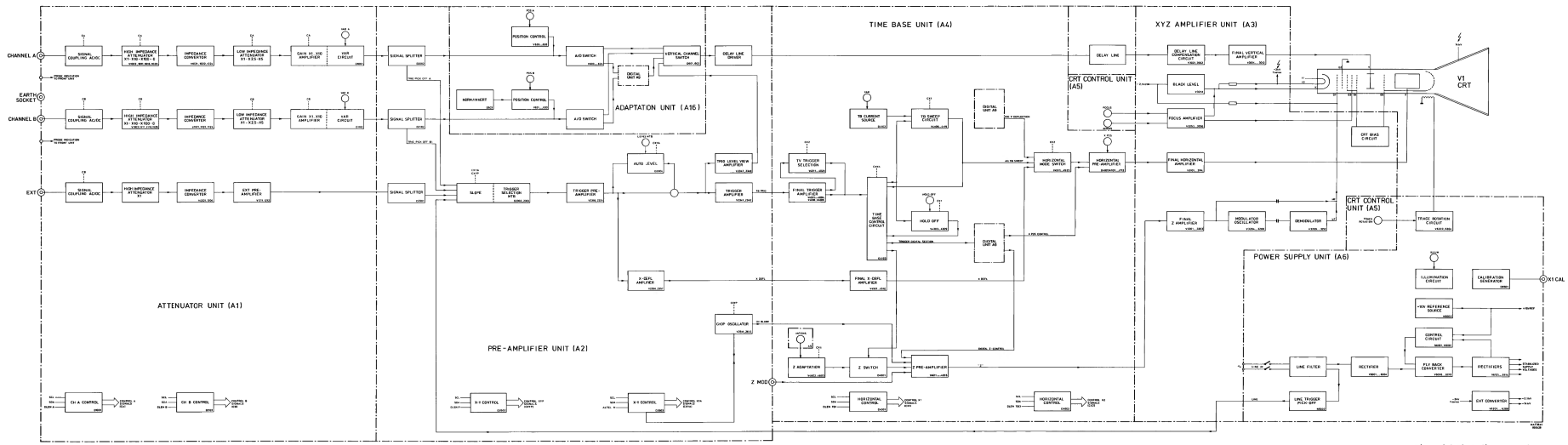


Figure 3.1 Block diagram, analog part

Signal name list:

The description of the digital unit A9 contains a list with the signal names used in that unit given in alphabetical order. After each name, a short signal description is given and also the signal source and the signal destination(s).
Only if the signal is generated on the unit itself, are the other units on which the signal is used (signal destination(s)) mentioned, otherwise a minus sign is filled in.

A number of power supply lines and ground lines are not mentioned on the signal name lists because they appear very often and because their function in obvious.

3.1.3 Location of electrical parts

The item numbers of C...., R...., V...., N...., D.... and K.... have been divided into groups which relate to the circuit and the printed-circuit board according to the following table:

Item number	Unit no.	Printed-circuit board
1000-1999	A1	Attenuator unit
2000-2999	A2	Pre-amplifier unit
3000-3999	A3	XYZ amplifier unit
4000-4999	A4	Time base unit
5000-5999	A5	CRT control unit
6000-6999	A6	Power-supply unit
7000-7999	A7	Front unit
8000-8999	A8	LCD unit
9000-9999	A9	Digital unit
600- 699	A16	Adaptation unit

3.2 BLOCK DIAGRAM DESCRIPTION (see figure 3.1 and 3.2)

3.2.1 Introduction

This block diagram description is based around all the important functional blocks and their interconnections. In order to assist in cross-reference with the circuit diagrams, the blocks include the item numbers of the active components they contain.
Furthermore, the blocks are grouped together per printed-circuit board, or a part of it. To facilitate reference, the names of the functional blocks are given in text in CAPITALS. Signal waveforms are also indicated at block interconnections where useful.
In this instrument almost all the switches (UP-DOWN controls, softkeys and potentiometer UNCAL switches) influence the oscilloscope circuits via a microprocessor (uP) system.

3.2.2 Attenuator unit (unit A1)

The vertical channels A and B for the signals to be displayed are identical. Each channel comprises an input SIGNAL COUPLING for AC/DC, a HIGH IMPEDANCE ATTENUATOR which gives signal attenuation of x1-x10 or x100, an IMPEDANCE CONVERTER, a LOW IMPEDANCE ATTENUATOR which gives signal attenuation of x1-x2,5 or x5 and a GAIN x1-x10 AMPLIFIER block, incorporated with the CONTINUOUS CIRCUIT. This block has a variable gain, influenced by the front-panel VAR control. The gain is also increased by x10 in order to obtain 2-5 and 10mV settings.

Similar to the vertical channels, the external channel attenuator also has an input SIGNAL COUPLING, HIGH IMPEDANCE ATTENUATOR and IMPEDANCE CONVERTER in line. However, the external channel has only x1 attenuation and no LOW IMPEDANCE ATTENUATOR. The output of the external channel is fed to both MTB and DTB EXT PRE-AMPLIFIERS.

All blocks that are capable of working in different modes are controlled by the control A or control B signals. These signals are generated by the CH.A CONTROL or CH.B CONTROL blocks under influence of the SDA and SCL signals that come from the MICROPROCESSOR.

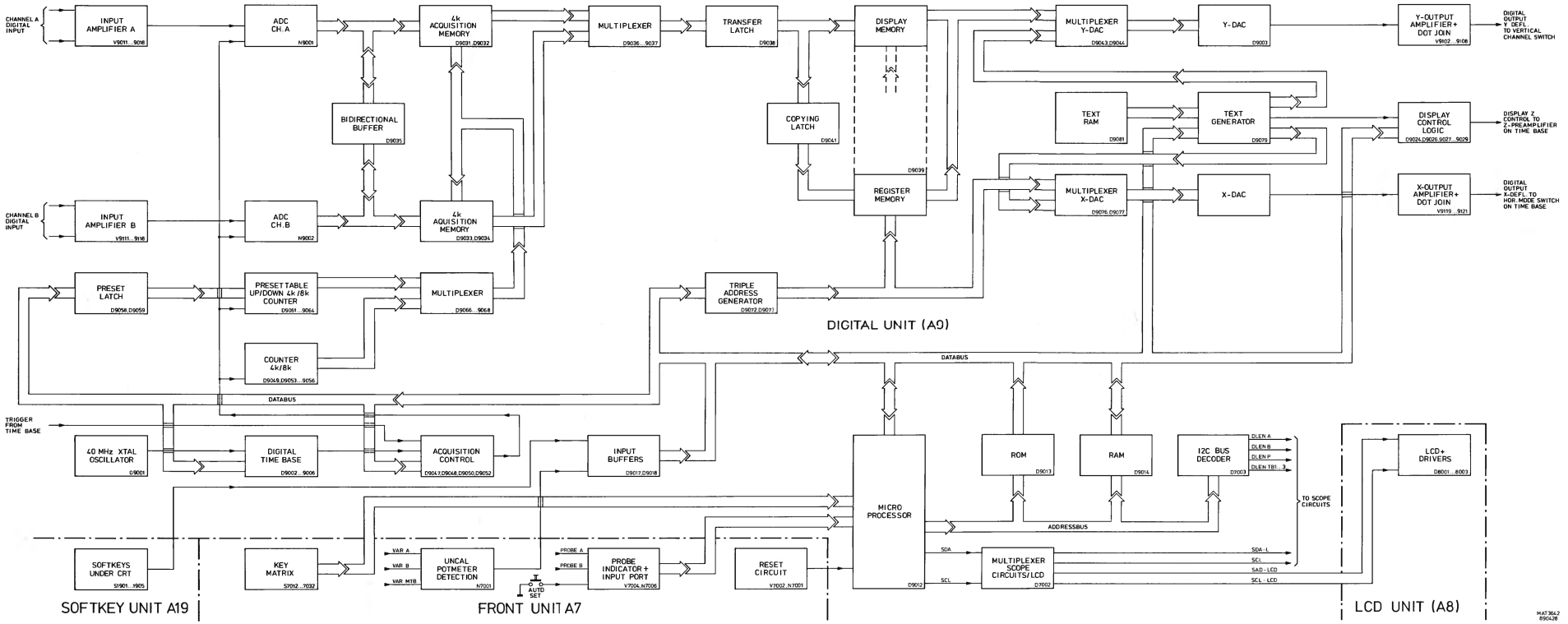


Figure 3.2 Block diagram, digital part

3.2.3 Pre-amplifier unit and adaptation unit (unit A2 and A16)

The pre-amplifier unit incorporates the signal splitters for the vertical channels A and B, the trigger level view amplifier, the trigger circuits for the time base and the chopper oscillator circuit. Next the adaptation unit is mounted as a separate p.c.b. on the pre-amplifier unit. All these functions are controlled by the control XYP and XYA signals, generated by the X-Y CONTROL blocks under influence of the SDA and SCL signals from the MICROPROCESSOR.

* Vertical channels A and B:

Both channels are completely identical and receive their input signals from the ATTENUATOR UNIT. This signal is applied to the SIGNAL SPLITTER, which has two outputs:

- one output is applied to the SLOPE/TRIGGER SELECTION for the time base triggering.
- A second output is routed to the adaptation unit.

On the adaptation unit, vertical shift of the displayed signal is achieved by the front-panel POSITION control.
Switching between the real time path and the digital storage path is obtained in the A/D SWITCH block. The digital circuit is given in figure 3.2 and described separately.
Next, the output of the VERTICAL CHANNEL SWITCH is routed via the DELAY LINE DRIVER to the DELAY LINE.
The TRIGGER LEVEL VIEW channel enables display of the time base trigger level and can be used to determine the trigger point of the signal.

* Trigger circuit:

The SLOPE/TRIGGER SELECTION block receives a trigger signal from one of the vertical channels A or B, from the EXT SIGNAL SPLITTER or from the LINE TRIGGER PICK-OFF.
Inverting of the trigger signal is controlled by the CXYA signals INVAM and INVBM to obtain the slope function.
Routed via the TRIGGER PRE-AMPLIFIER, block the signal is split up into different paths:

- after summation of the LEVEL signal, direct to the TRIGGER AMPLIFIER
- to the AUTO LEVEL block. This block contains the different trigger facilities and levelling of the trigger signal is influenced by the front-panel LEVEL control. The output of this path is routed again to the summation point to influence the direct trigger signal.
- to the X-DEFL AMPLIFIER for X-deflection facility. This block incorporates a phase correction circuit for the X-Y display.

The TRIGGER AMPLIFIER feeds the trigger signal to the time-base unit. The trigger signal from the summation point is also routed via the TRIGGER LEVEL VIEW AMPLIFIER to the vertical CHANNEL SWITCH stage to display the trigger point.

* Chopper oscillator circuit:

A square-wave signal for chopper blanking and vertical switching is generated in the CHOP OSCILLATOR. For chopper blanking the signal is routed to the Z PRE-AMPLIFIER on the time-base unit.

3.2.4 Time-base unit (unit A4)

This unit incorporates the time-base (TB), the horizontal amplifier and the Z amplifier circuit. All functions are controlled by the CX1 and CX2 signals, generated by the HORIZONTAL CONTROL CIRCUIT blocks.

* Time-base (TB):
The trigger signal can be either routed via the FINAL TRIGGER AMPLIFIER to the TIME-BASE CONTROL CIRCUIT or first routed via the TV TRIGGER SELECTION for the TV trigger coupling. When in the AUTO mode, in the absence of trigger signals, the time base will be free running.

The CURRENT SOURCE applies the sawtooth charging current to the sweep circuit. This block generates the time base sawtooth signal, which is routed to the HORIZONTAL DISPLAY MODE SWITCH..

The HOLD OFF and the DIGITAL UNIT blocks are also under control of the TIME BASE CONTROL CIRCUIT. Hold off time is varied by the front-panel HOLD OFF control. The output of the HOLD OFF block is routed to the TIME-BASE CONTROL CIRCUIT again. The signal going to the DIGITAL UNIT triggers the digital signal acquisition.

The ALTCLN-pulse is applied to the PRE-AMPLIFIER UNIT.

3.2.5 XYZ unit (unit A3)

This unit comprises the final amplifiers for the vertical (Y) and horizontal (X) deflection and for the blanking (Z) circuit. In addition to this, the CRT control circuits are also incorporated in the unit.

* Final vertical amplifier:

The output signal from the pre-amplifier unit is first routed via the DELAY LINE to give sufficient delay to ensure that the steep leading edges of fast signals are displayed and then fed to the DELAY LINE COMPENSATION. This block compensates the signal fordistortion originating in the DELAY LINE before it is applied to the FINAL VERTICAL AMPLIFIER. The output of the FINAL VERTICAL AMPLIFIER feeds the vertical deflection plates of the CRT.

* Final horizontal amplifier:

The horizontal deflection signal is routed to the FINAL HORIZONTAL AMPLIFIER, the output of which feeds the horizontal deflection plates of the CRT.

* Blanking circuit:

The output signal from the Z PRE-AMPLIFIER of the time-base unit, that determines trace blanking or unblanking and modulation is routed to the FINAL Z-AMPLIFIER. After amplification the blanking signal is split into two paths:

- the h.f. signals are fed via a high voltage capacitor to grid G1 of the CRT.
- the l.f. signals are used to modulate the amplitude of an oscillator wave-form, which then passes via another high voltage capacitor and is demodulated in the DEMODULATOR block to retrieve the original signal.

Note that the original h.f. and l.f. signals are again recombined on the grid G1.

* CRT control circuits:

The FOCUS AMPLIFIER block is influenced by both front-panel FOCUS and INTENS controls to provide a focus that is independent of the intensity, and drives the focusing grid G3 of the CRT.

The -100 V BLACK LEVEL block provides the correct presetting of the cathode voltage.

The CRT BIAS gives a d.c. voltage to the grids G4 and G5 to provide an optional adjustment for geometry and astigmatism.

3.2.6 Power supply unit

The mains input voltage is filtered and then applied to the RECTIFIER block to obtain a d.c. voltage source. Another output of the LINE FILTER block is routed via the LINE TRIGGER PICK-OFF and serves as a MTB LINE trigger signal. The rectified mains source is routed to the FLYBACK CONVERTER, which generates the necessary voltages for the oscilloscope circuits. Each supply voltage is rectified in the RECTIFIERS block.
The LOW-voltage supplies are stabilized by the CONTROL circuit to the converter.
The +10 V REF supply serves as a low-voltage reference and is generated in the +10 V REFERENCE source block. This reference voltage is also fed to the different circuits on the power supply or in the oscilloscope.

The EHT CONVERTER generates the -14 kV for the post-accelerator anode of the CRT and the -2 kV for the cathode circuits.

* Auxiliary circuits:

The CALIBRATION GENERATOR generates the CAL voltage, which is applied to the output socket X1. The CAL voltage has a square-wave of 1,2 V p-p level with a frequency of 2 kHz.

The ILLUMINATION CIRCUIT determines the amount of current passed to the graticule illumination lamp of the CRT, controlled by the ILLUM control on the front-panel.

The TRACE ROTATION CIRCUIT determines the strength and sense of the current passed to the trace rotation coil around the neck of the CRT. The current is influenced by the front-panel screwdriver-operated TRACE ROT control.

3.2.7 Digital memory and control circuits (unit A7, A8, A9 and A19)

Introduction.
The blockdiagram of the digital sections can roughly be split up into three main parts. These parts are:
- Signal acquisition: this section captures signal samples and places them in the acquisition memories.
- The memory and display part are used to store the signal and to display it on the CRT screen.
- The control section that is based upon a microprocessor takes care that the signal display and acquisition function correctly. Moreover it reads all the instrument's knobs and controls all analog and digital circuits.

The digital parts are mainly concentrated on the large digital unit A9. A small part is present on the front unit A7 and the LCD unit A8. The softkey unit A19 is located under the CRT and only incorporates five softkeys.

Signal acquisition.
The channel A(B) signals that are coming from the adaptation unit A16 are applied to the INPUT AMPLIFIERS A(B). These blocks feed the analog-to-digital converters ADC CHANNEL A and ADC CHANNEL B. The digitised signals of channel A and B can be loaded into two 4K ACQUISITION MEMORY blocks. In case of dual channel mode, each channel is loaded into one 4K memory. In case of single channel operation, the full 8K memory capacity is available for one channel. The BIDIRECTIONAL BUFFER makes it possible that the ADC-output of the selected single channel can reach the input of both 4K memories.

The addresses for the two 4K ACQUISITION MEMORIES are originating from two counters. COUNTER 4K/8K is only able to count upwards and has a range of 4K or 8K addresses. The PRESETTABLE UP/DOWN COUNTER has also a range of 4K/8K. It can also count up or down and can be preset by the MICROPROCESOR via the block PRESET LATCH. Depending on the state of the MULTIPLEXER, the address of one of the two counters is addressing the 4K ACQUISITION MEMORIES. The possible modes are explained more in depth during the circuit description; also the trigger delay mode is explained then.

The acquisition of signal samples is synchronised by the DIGITAL TIME BASE circuit. This circuit is based upon a 40MHz XTAL OSCILLATOR that is followed by the DIGITAL TIME BASE. The DIGITAL TIME BASE is put in the appropriate position via the ADDRESSBUS of the MICROPROCESSOR. The output signal of the DIGITAL TIME BASE is applied to the ACQUISITION CONTROL block. Also this block is controlled by the MICROPROCESSOR and it takes care that the ADC's take signal samples at the correct moment and that these samples are placed in the appropriate part of the ACQUISITION MEMORIES. The trigger pulse that originates from the TIME BASE is also applied to the ACQUISITION CONTROL.

Memory section and display part.
The contents of the two 4K ACQUISITION MEMORIES can be transferred to the DISPLAY MEMORY. This happens at a particular moment after a trigger. The transfer occurs via the TRANSFER LATCH. The contents of the DISPLAY MEMORY can be copied via the COPYING LATCH into the REGISTER MEMORY. This last memory can be used to store waveforms for reference purposes.

The addressing of the DISPLAY MEMORY and the REGISTER MEMORY is done by the TRIPLE ADDRESS GENERATOR. This block is controlled by the MICROPROCESSOR and contains three separate address generators. They have the following purposes:
- The addressing of the display memory during the information transfer from ACQUISITION MEMORIES to the DISPLAY MEMORY.
- The addressing of the DISPLAY/REGISTER MEMORY during the transfer of information between these memory blocks.
- The addressing of the DISPLAY and REGISTER MEMORY during the display on the CRT screen of their contents. The contents of the addressed memory locations is applied to the vertical Y DAC and then to the Y OUTPUT AMPLIFIER. The address itself is applied to the horizontal X DAC and then to the X OUTPUT AMPLIFIER.

The X and Y OUTPUT AMPLIFIERS also incorporate a DOT JOIN facility. This means in the DOT JOIN mode a decrease of the speed of these amplifiers because a low pass filter is added. This has the result that the move from one dot to the next one is smoothed.

The input of the Y DAC and the X DAC are connected with two-position multiplexers. They are named MULTIPLEXER Y DAC and MULTIPLEXER X DAC. In one position of the multiplexer, the contents of the DISPLAY/REGISTER MEMORY is displayed. In the other position text and cursors are displayed: this is generated by the TEXT GENERATOR. This block is integrated in one IC. The kind of text to be generated is given by the MICROPROCESSOR. This text is stored into the TEXT RAM (Random Access Memory) that belongs to the TEXT GENERATOR.

Control section.
The heart of this part is formed by the MICROPROCESSOR with belonging ROM (Read Only Memory) and RAM (Random Access Memory). Via the block INPUT BUFFERS, the MICROPROCESSOR reads the softkeys under the CRT and also the UNCAL position of VARiable A, VARiable B and VARiable MTB. The MICROPROCESSOR directly reads the KEY MATRIX at the front unit A7. The RESET CIRCUIT on unit A7 initiates the MICROPROCESSOR when switching the power on.

The MICROPROCESSOR controls many circuits inside the oscilloscope. The blocks on the digital unit that are under control of the MICRO-PROCESSOR are already explained. They are all connected with the databus or parts of it. Also the LCD and the analog scope circuits are under microprocessor control. For this purpose the so-called I2C bus is used. This is a bus consisting of two signal wires: the data line SDA (Serial DAta) and the synchronisation line SCL (Serial CLock). The I2C bus lines are switched to either the LCD (as SDA-LCD and SCL-LCD) or the analog scope circuits. This selection is made via the MULTIPLEXER SCOPE CIRCUITS/LCD. The analog scope circuits incorporate many control blocks that are all connected to the SDA and SCL lines of the I2C bus. The control blocks are separately addressed via the I2C BUS DECODER. If e.g. output DLEN A (Data Latch ENable A) is active, the control block of channel A on the attenuator unit accepts the data from SDA/SCL. The result is for instance that the channel A attenuator switches to another input sensitivity. Identical to this the signals DLEN B, DLEN P and DLEN TB 1...3 activate the control blocks on respectively the channel B attenuator, the preamplifier and the time base.

4. ATTENUATOR UNIT (A1)

4.1 VERTICAL ATTENUATORS

The A and B channel attenuators are identical: therefore only channel A is described.

All relay and FET switches are controlled by the microcomputer via the I^2C bus. The IC D1001 converts this serial DATA into the parallel control signals for all relay or FET switches. A list of the control lines for all attenuator settings is given in the table below.

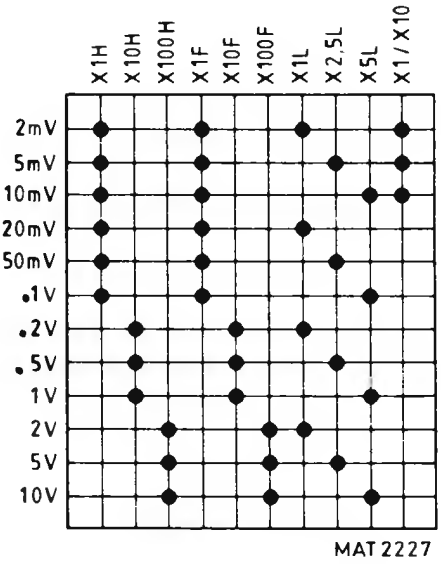


Figure 4.1 Table of attenuator settings

The channel A attenuator consists of in five stages:

Input coupling, where depending on the relay K1001 position, the input signal can either be d.c.-coupled (relay activated) or a.c.-coupled (relay not activated).

High impedance attenuator with three attenuator stages for the x1, x10 and x100 attenuation. The 1.f. part of each stage is split via a resistor divider and routed via N1001 and V1019 to the output of this stage, where it is re-connected with the h.f. part of the input signal. Potentiometers R1036 (TRACE jump) serves as a offset compensation for N1001.

	RELAY	FET	TRIMMER FOR L.F. SQUARE WAVE	L.F. RESISTOR DIVIDER
x1	K1004	V1011	C1033	--
x10	K1003	V1006	C1029	R1007-R1011
x100	K1002	V1003	C1023	R1019-R1004

Note that, when "0" (GND-A) is selected, the output is connected to ground via FET V1016 and all other relay- and FET switches are switched off.

The impedance converter serves as an inverting buffer circuit for the high impedance attenuator. For the l.f.-feedback the output signal of this stage is routed to the l.f. summation point N1001-2.

The low impedance attenuator reduces the gain by x1, x2.5 and x5, depending on which relay is activated.

	RELAY	RESISTOR DIVIDER
x1	K1006	--
x2.5	K1007	R1053 vs R1056, R1057 and R1058
x5	K1008	R1053, R1056 and R1057 vs R1058

The continuous circuit (D1061), the differential input voltages of which are fed to pins 4 and 5.
This stage comprises the following functions:

- Continuously variable control (pin 11).
- Gain x1 (pin 2 and 3) with offset adjustment R1064 and gain adjustment R1069.
- Gain x10 (pin 6 and 7) with offset adjusting R1072 and gain adjustment R1076.
- x1/x10 control (pin 10) to select the 2,5 and 10 mV/DIV settings.

The differential output current from pin 13 and pin 14 is routed via a common-base circuit V1063, V1064 and applied to the pre-amplifier unit.

4.2 EXTERNAL INPUT

The external input can be subdivided into four stages:

Input coupling, basically similar to the ch.A input coupling.

High impedance attenuator for the x1 attenuator only, where the l.f. square-wave can be adjusted with trimmer C1206. The l.f. part is routed to the summation point N1201-2. R1217 serves as an offset compensation for N1201. For l.f.-feedback the output of the impedance converter is also routed to this summation point.

Note that the output of this stage is also a reconstituted version of the input signal.

Impedance converter, is basic similar to the ch.A impedance converter.

The differential amplifier V1211, V1212 converts the voltage from emitter-follower V1209 into the differential current signals EXT+ and EXT-. This signal is applied to the pre-amplifier unit and serves as external trigger signal or as an external deflection signal.
The current for this stage is applied from current source V1213.

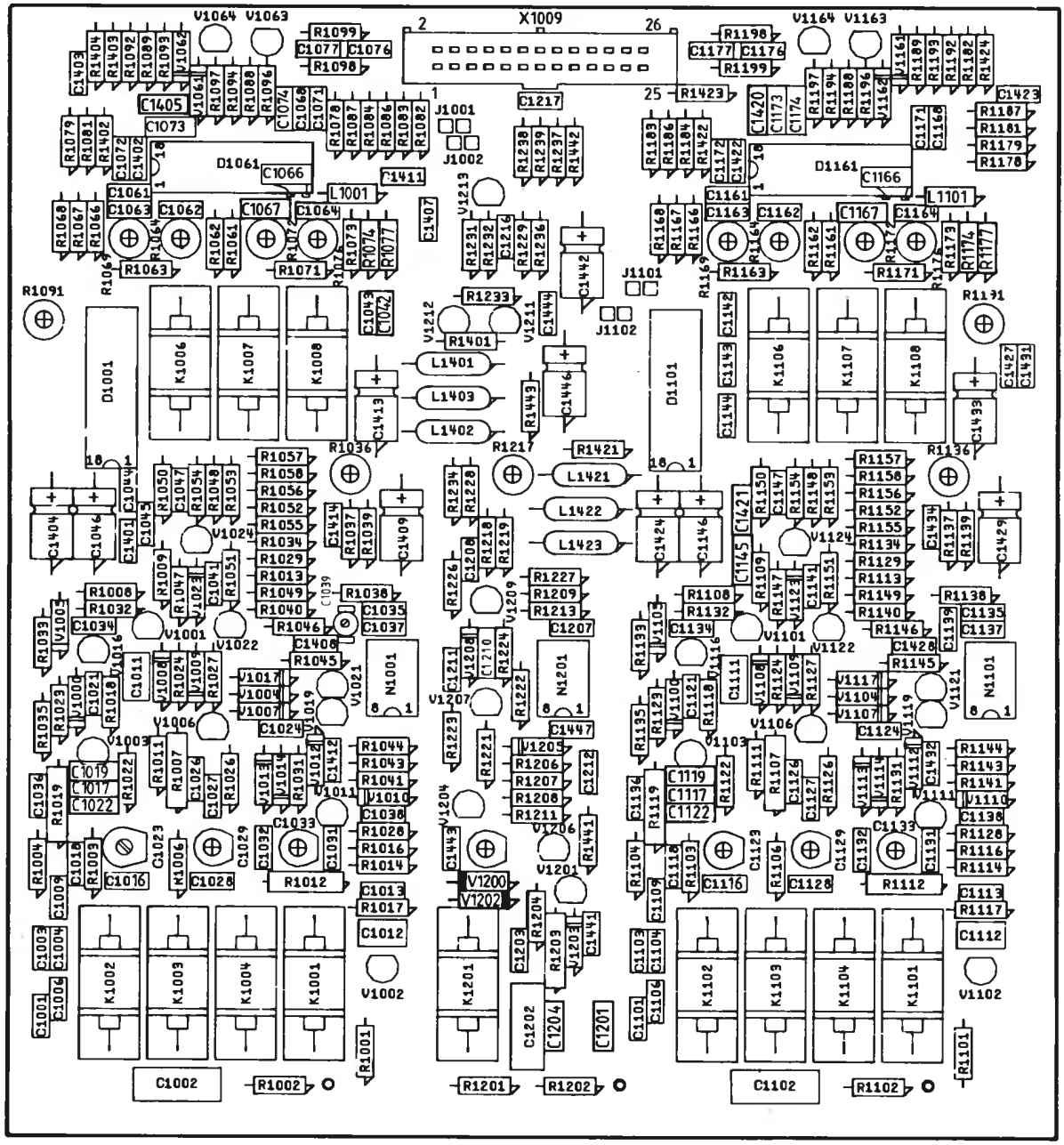


Figure 4.2 Attenuator unit p.c.b.

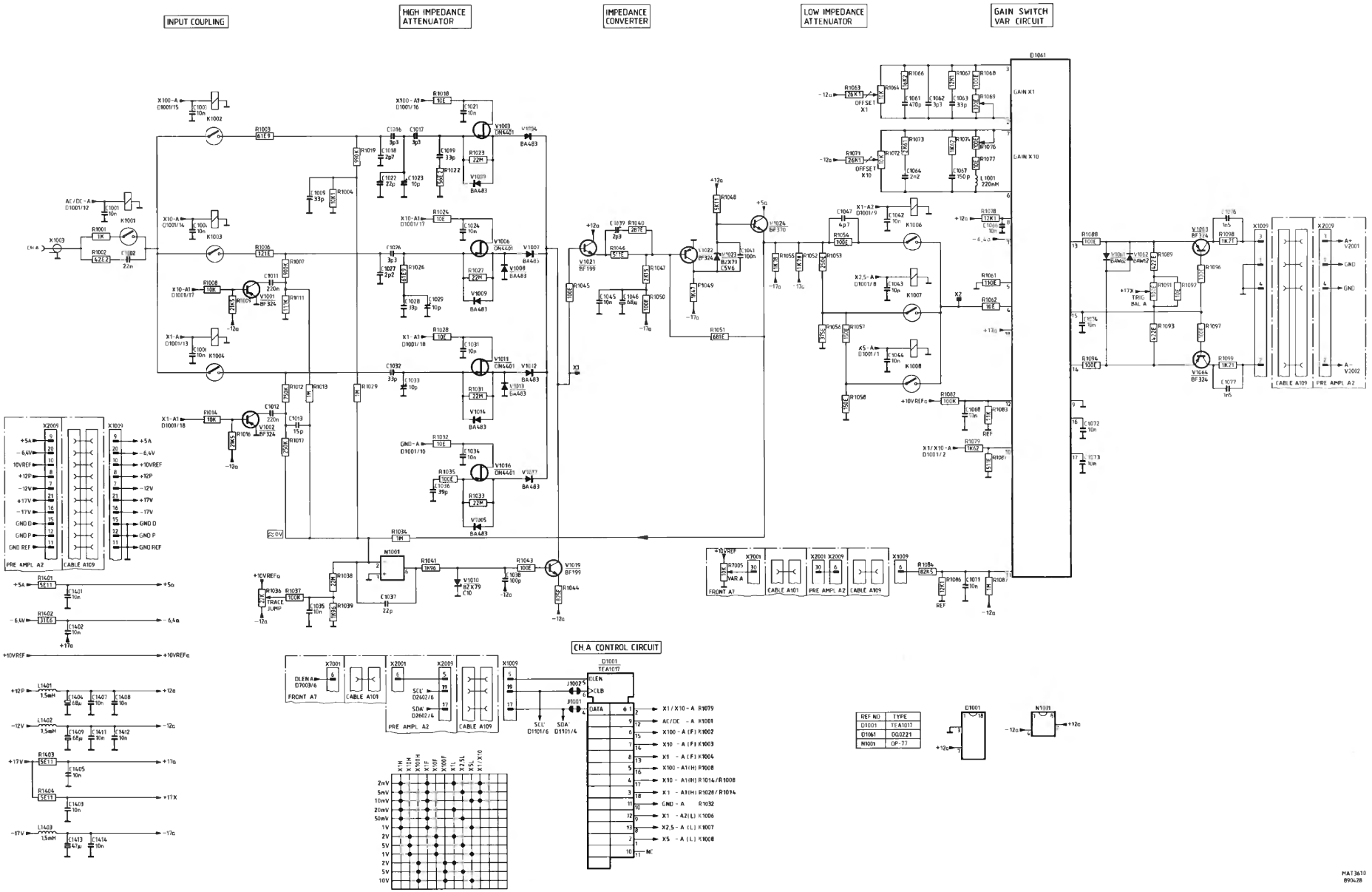


Figure 4.3 Circuit diagram of attenuator, ch.A

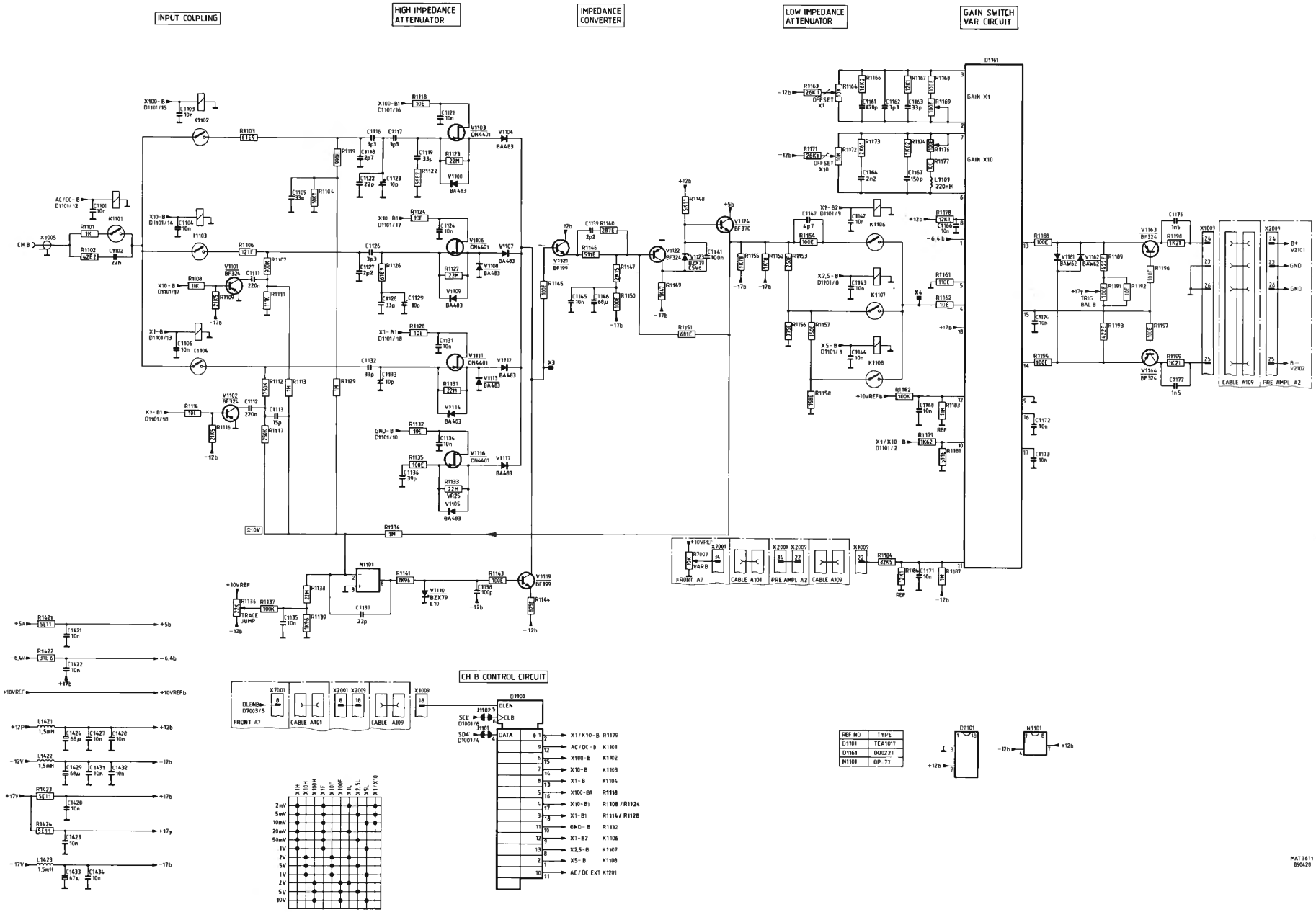


Figure 4.4 Circuit diagram of attenuator, ch.B

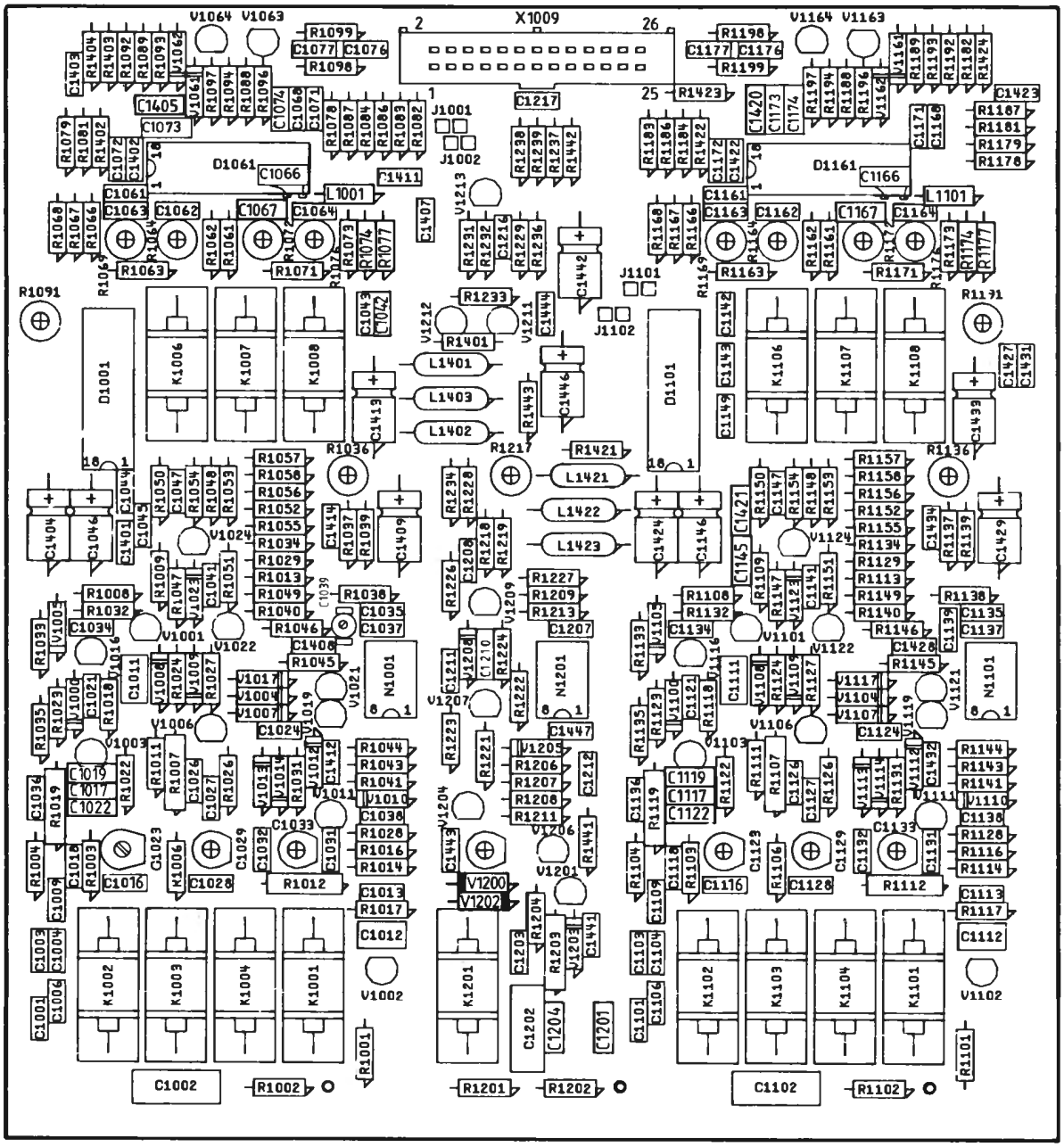


Figure 4.5 Attenuator unit p.c.b.

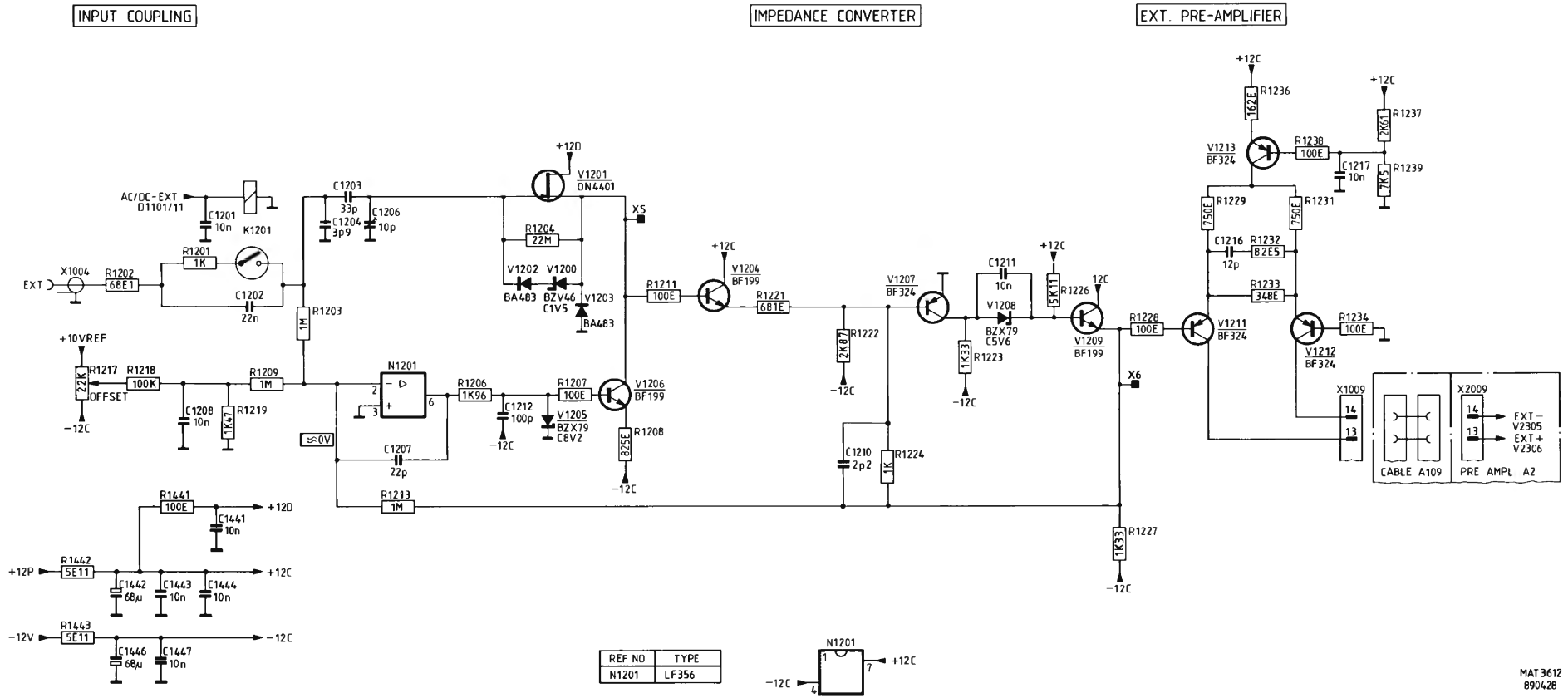


Figure 4.6 Circuit diagram of attenuator, EXT

5. PRE-AMPLIFIER UNIT (A2)

The pre-amplifier unit consists of:

- Vertical pre-amplifier
- Trigger pre-amplifier
- Pre-amplifier control, including CHOPPER oscillator

Next, the adaptation unit A16 is mounted on this board.
This unit is described separately in chapter 17.

All control pulses for this unit are generated by the pre-amplifier control circuit, via the I^2C bus (see Section 5.4).

5.1 VERTICAL PRE-AMPLIFIER

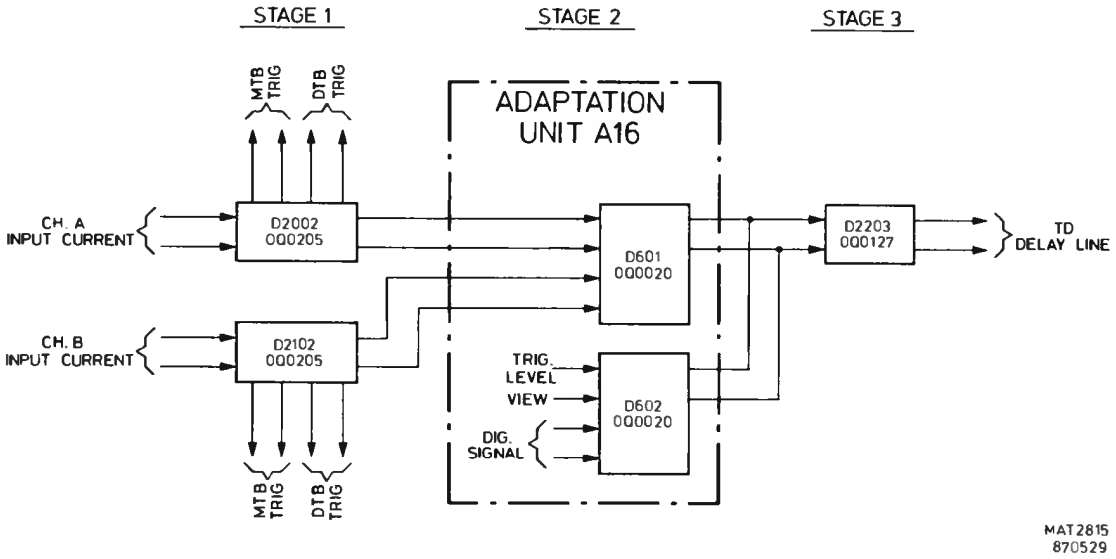


Figure 5.1 The three stages of the vertical pre-amplifier

The vertical pre-amplifier consists of three stages.

The signal splitter (Q0205) receives its input signal for channel A (B) from the attenuator unit and copies this signal into two identical differential output current signals for:

- Vertical deflection (pin 7 and 10)
- Time Base triggering (pin 5 and 12), refer to section 5.2.

The output of pin 7 and 10 is applied to the adaptation unit A16.

Stage 2 (unit A16), refer to the description of A16.

Stage 3 (D2203) serves as delay line driver where the output current of both OQ0020's is converted into voltage signal applied to the delay line. The current for this stage and for the OQ0020's D601 and D602 on adaption unit A16 is supplied via R2231 and R2246.
The current regulation for the common-mode circuit is achieved by transistor D2203 (12, 13, 14).

5.2 TB TRIGGER PRE-AMPLIFIER

Trigger possibilities are:

	Signal		Selected by:		Inverted by:	
	name	routed to	name	routed to	name	routed to
ch. A	TRAM+, TRAM-	D2302(3,4)	AM	D2302(10)	INVAM	D2302(2)
ch. B	TRBM+, TRBM-	D2302(5,6)	BM	D2302(11)	INVBM	D2302(7)
EXTERNAL	EXT-, EXT+	D2303(3,4)	EXTM	D2303(10)	INVAM	D2303(2)
line	LINE	D2303(5)	LNM	D2303(11)	INVAM	D2303(7)

D2301 serves as a signal splitter and receives its input signal from the attenuator unit. This input current signal is copied into identical differential output current signals for EXT MTB signal (pin 6 and 11)

The symmetrical output currents from D2302 (13, 14) and D2303 (13, 14) are converted into a symmetrical voltage again in the common-base circuit V2316, V2319 followed by a shunt feedback circuit V2318 and V2321. Note that the sensitivity at the collectors of V2318 and V2321 is 110 mV/DIV.

At this point the signal path is divided into:

- a trigger path, fed to both V2333 and V2334, where depending on the current to the base, levelling of the trigger signal is obtained. Two separate series feedback circuits take care of voltage-to-current conversion:
  * V2341 and V2342 for time-base triggering.
    The trigger output signal, TRIGM- and TRIGM+ are fed to the time-base unit A4.
  * V2347 and V2349 for trigger level view.
    This symmetrical output can be balanced by potentiometer R2407. The TRIGV+ and TRIGV- signals are fed to D602/3,4 on the adaptation unit A16.

Integrated circuit D2304 serves as an auto level circuit. The following functions are possible:

a. Peak-peak

In this case the amplitude of the trigger signal applied to D2304 (3,7) is measured by peak-peak detectors on D2304 (2,4,6,8). The output current from D2304 (14,15) is dependent on the peak-peak level and is adjustable with the LEVEL control R7012, connected to D2304(1).

b. Triggering

In this case the level range is 16 div. The level is adjustable with R7012 and the current variation on D2304 (14,15) can be varied between +or- 0,6mA.

c. TV triggering

The level control is made ineffective. In TV triggering, the LEVEL must be set to a fixed value. This is done by applying a high level current to pin 1 via diode V2326.

d. Auto

In auto the signal LEVEL NUL is high and via diode V2325 the output level D2304 (15) is asymmetrical with output level D2304 (14). Thus the maximum signal amplitude is 2 Vp-p.

- an external deflection path, routed via the series feedback circuit V2356 and V2357, the X DEFL+ and X DEFL- signals are fed to the time base unit A2.
  R2416, R2422 and C2350 gives phase correction for the X-Y display.

5.3 PRE-AMPLIFIER CONTROL

The pre-amplifier control converts the data from the I^2C bus (SDA and SCL), derived from the microcomputer, into the control pulses for the pre-amplifier unit. To eliminate interference the SDA and SCL lines can be switched off via D2601.

This integrated circuit serves as a digital switch, controlled by the VERT IIC line. Logic high connects the outputs D2601(4,14,15) to the input "1" contact (switched on); logic low connects the outputs to the "2" contact (switched off) and gives SDA a logic low level and SCL a logic high level.

When D2601 is switched on, the serial data information is converted into parallel control pulses via D2602 and D2603, provided that D2602 is enabled (D2602-5 is high). The control lines are active when the level of the line is high.

Output Q12-D2602(9) serves as a power up not line for D2603: when the oscilloscope is in the power-up routine, Q12 is high and resets D2603. After the power-up routine, Q12 goes low and enables D2603.

Integrated circuit D2603 relieves the microcomputer of a number of such functions as:

- chop/alt
- trigger select
- time-base select (fed to time base unit A4)

Adaptation of this I.C. to the oscilloscope version is made by the AD0 and AD1 inputs D2603(15,16).
For this oscilloscope, AD0 must be HIGH and AD1 must be LOW.

Timing for alternate and chopped mode is derived by the ALTCLN and CHOPCL pulses.

The chopper oscillator formed by V2611 and V2612 supplies a square wave voltage of 1,5 Vp-p with a frequency of 1 MHz.

This frequency is defined by two current loops:

- I1 is determined by: V2612(c-e), C2611, R2627 and R2625.
- I2 is determined by: V2611(c-e), C2611, R2628 and R2625.

The duty cycle (I1/I1+I2) is 12% approx.

The square wave on the collector of V2612 serves as a chopper clock pulse for D2603 and gives a 500 kHz display for 2 channels CHOP, 333 kHz display for 3 channels CHOP and 250 kHz for 4 channels CHOP (A-B-TRIG VIEW-ADD).

Note that D2603(8) serves as the chopper switch, which is high when the CHOP softkey is depressed.

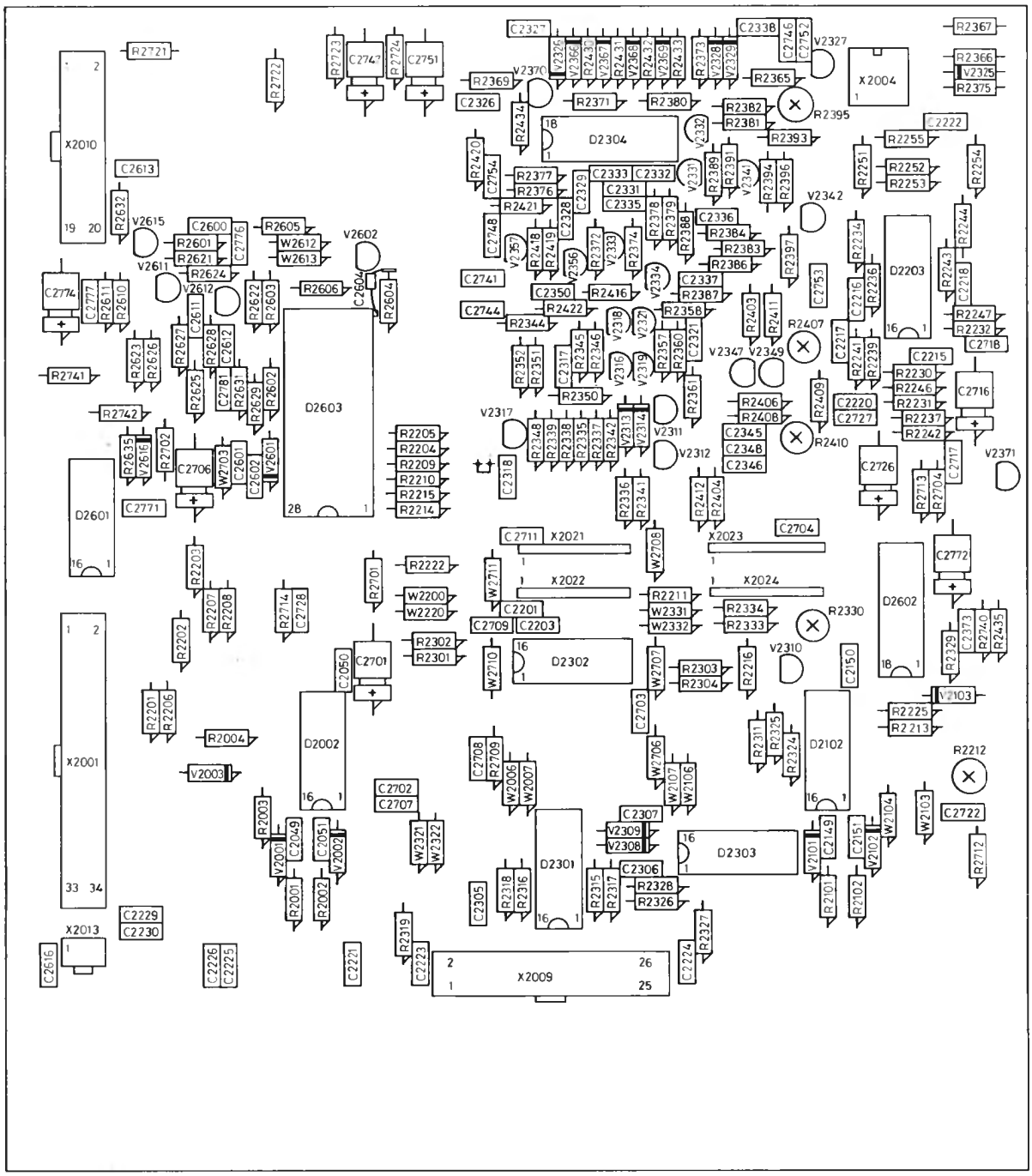


Figure 5.2 Pre-amplifier unit p.c.b.

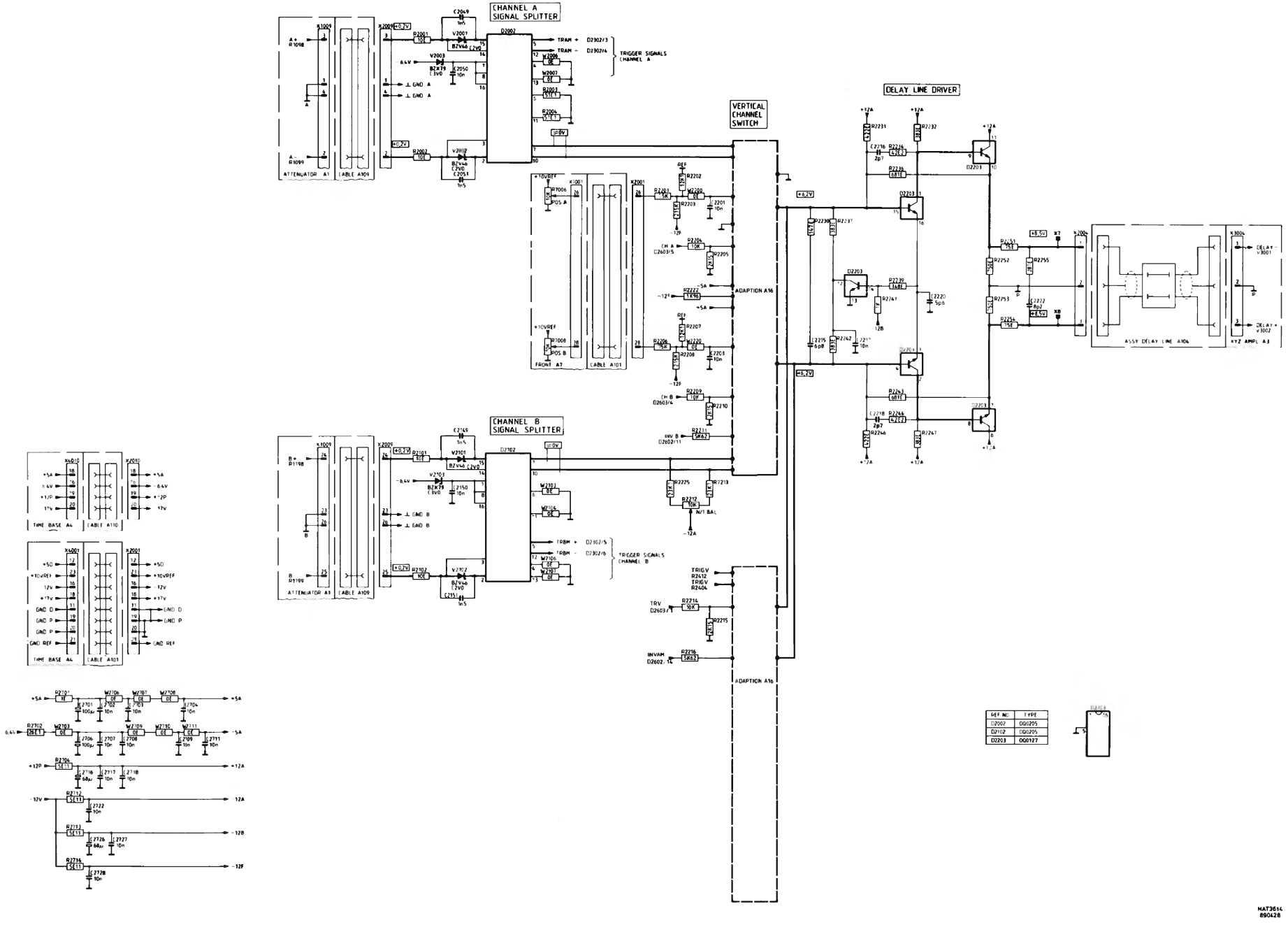
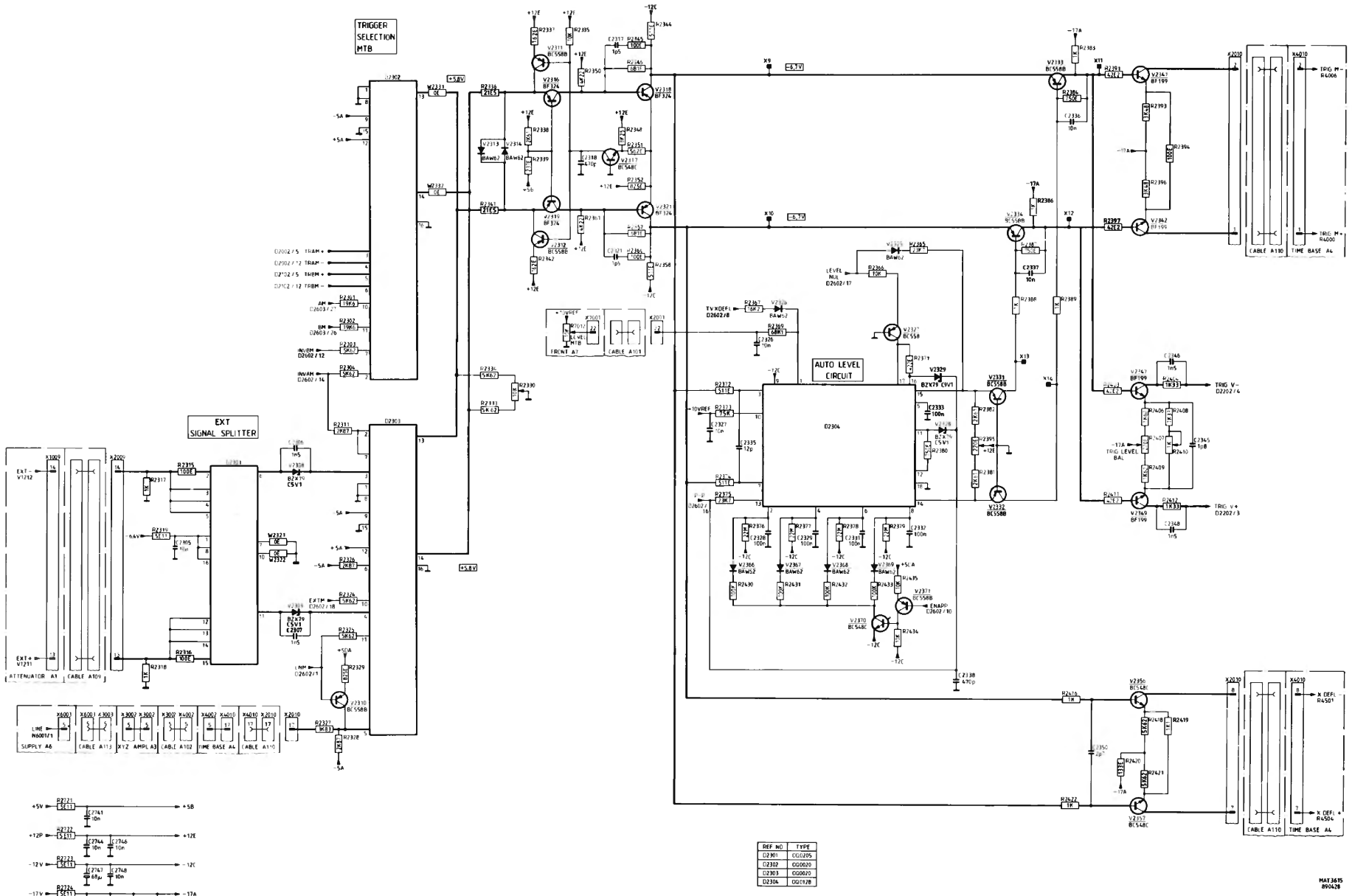
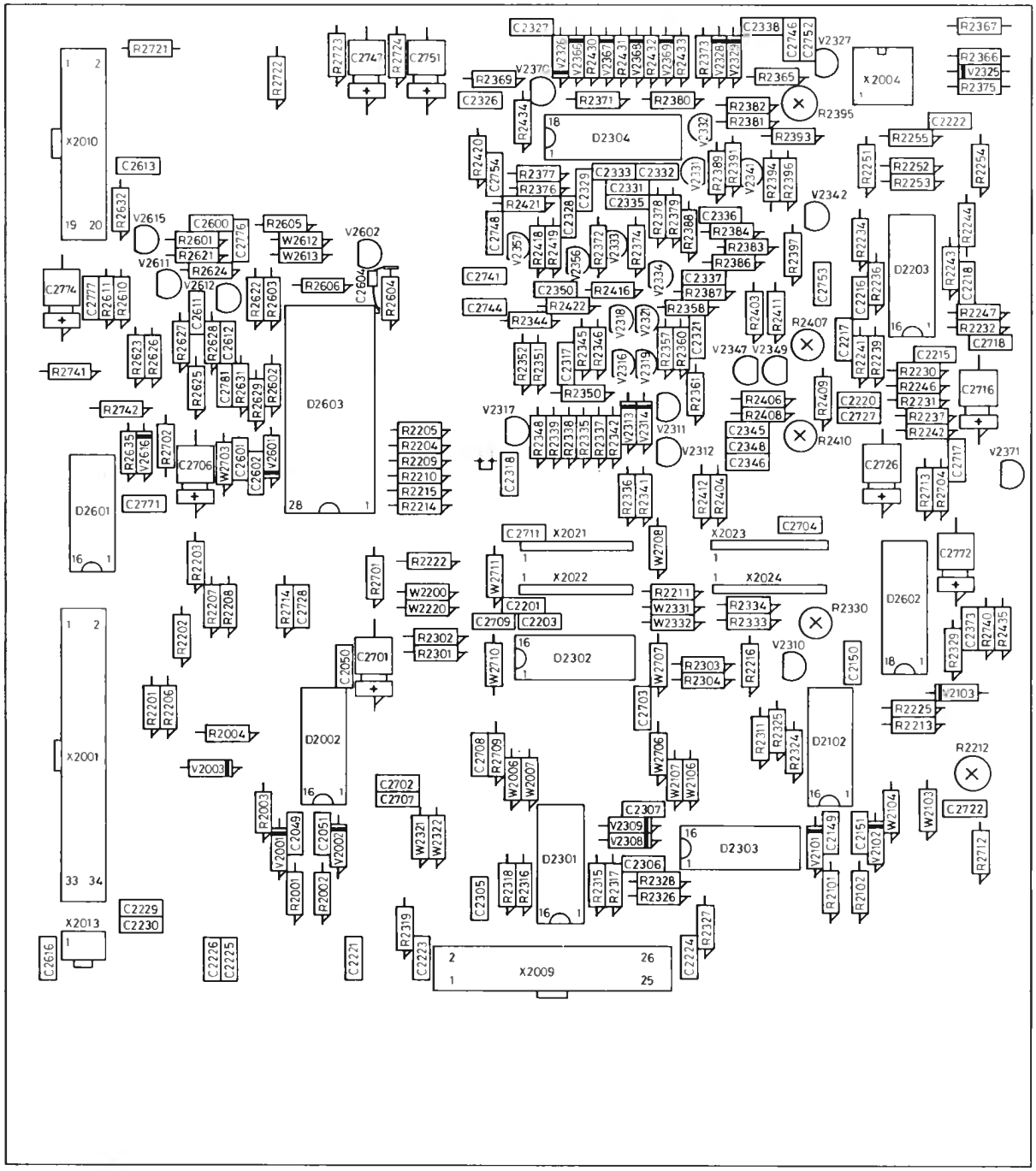


Figure 5.3 Circuit diagram of pre-amplifier, channel switch and delay line driver



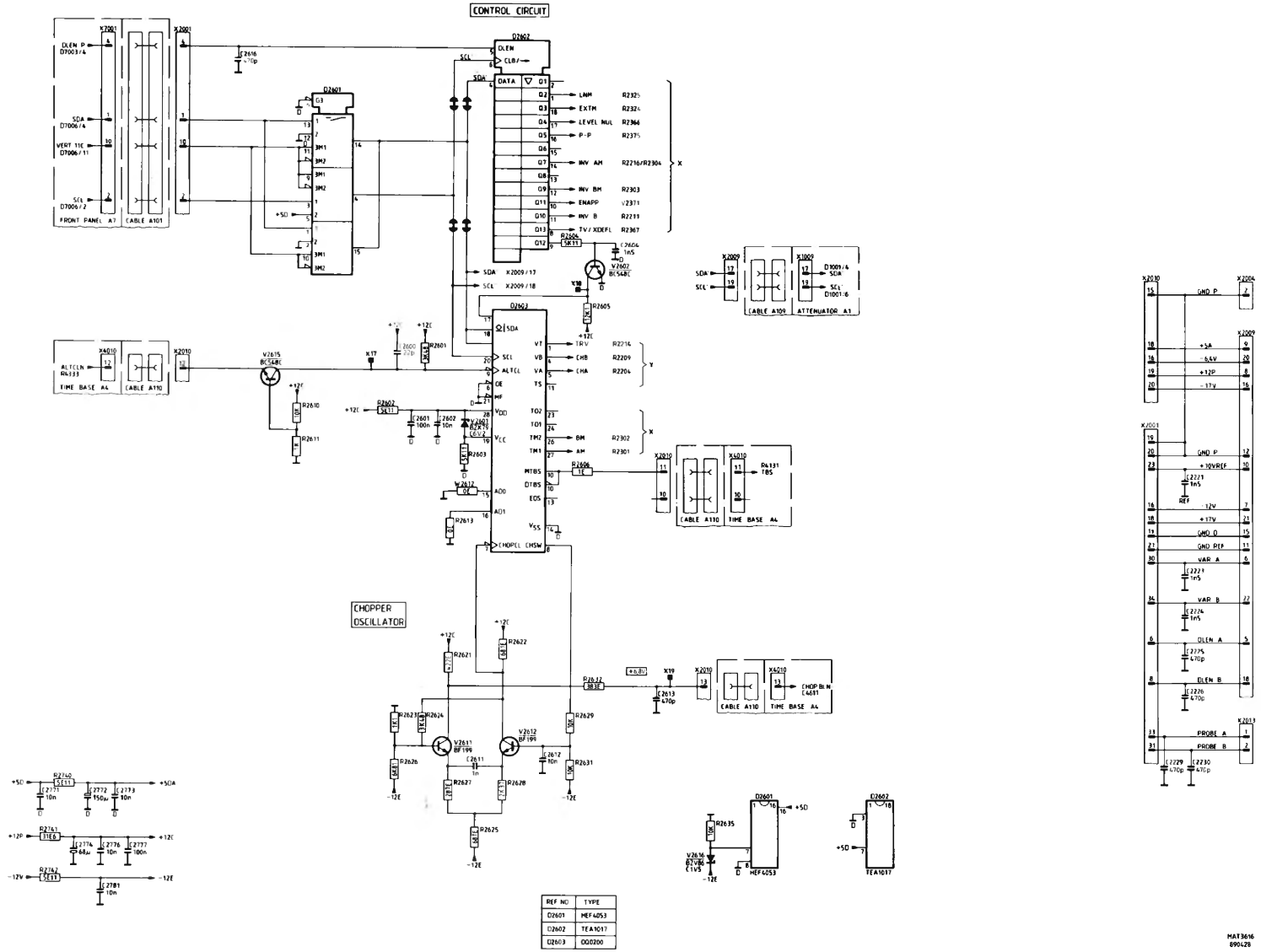
REF NO	TYPE
D2301	QQ0205
D2302	QQ0020
D2303	QQ0020
D2304	QQ0128

Figure 5.4 Circuit diagram of pre-amplifier, trigger switch



MAT 3613
890428

Figure 5.5 Pre-amplifier unit p.c.b.



REF NO	TYPE
D2601	MEF4053
D2602	TEA1017
D2603	OQ0200

MAT3616
890428

Figure 5.6 Circuit diagram of pre-amplifier, logic control

6. XYZ-AMPLIFIER UNIT (A3)

6.1 INTRODUCTION

Unit A3 incorporates two separate pcb's which are connected via a flatcable. One pcb includes among other things the CRT socket and is connected at the rear of the CRT. The other pcb comprising the proper final X and Z amplifiers is situated above the Cathode Ray Tube (CRT). For ease of description, unit A3 is described as one unit.

The XYZ-amplifier unit consists of:

- Final vertical (Y) amplifier.
- Final horizontal (X) amplifier.
- Final unblanking (Z) amplifier, incl. CRT.

6.2 FINAL VERTICAL (Y) AMPLIFIER

The final Y-amplifier receives its signal from the delay line and supplies the correct vertical signal to the Y-deflection plates of the CRT. For this the signal is processed in four stages:

- V3001, V3002 is a series feedback amplifier, including a delay line compensation network and potentiometer R3007 that controls current source V3003 for correction of any unbalance in the Y-deflection plates of the CRT. These circuits are connected between the emitters of both transistors V3001 and V3002.
  In this stage the input voltage is converted into a current signal.
- V3004, V3006 is a shunt feedback amplifier, which gives a voltage signal to the next stage.
- V3008, V3009 is a series feedback amplifier, including a final RC-correction network and potentiometer R3038 for gain adjustment to compensate the different CRT sensitivities. V3007 supplies a constant current of 60 mA, i.e. 30 mA for each half. Note that the output again supplies a current signal.
- V3011, V3012 is a common-base amplifier for buffering the final Y-amplifier to the Y-deflection plates. The maximum amplitude on each deflection plate is: 30 mA x 655 E = 20 V approx.

6.3 FINAL HORIZONTAL (X) AMPLIFIER

The input current for X-deflection is obtained from the time-base unit (ref: X- and X+) and processed in three stages, with circuits in the following configurations:

- V3101, V3102 is a common-base amplifier. The current "I" on the collector of both transistors determines the voltage across R3102 and R3116. This voltage is about 1,5 V p-p and feeds the next stage.
- V3103, V3106 is a series feedback amplifier, including an RC-correction network for optimum linearity of the trace and potentiometer R3118 for xl amplifier adjustment, mounted between the emitters of both transistors. V3104 serves as current source.

- V3112, V3114 are connected as a shunt feedback amplifier, with resistors R3126 and R3134 as the feedback resistors. The transistor source are emitter followers V3109, V3111. This circuit serves as the actual final amplifier, which converts the deflection current into the proper deflection voltage for the X-deflection plates of the CRT. Transistors V3108, V3116 supply the bias current for the circuit.

6.4 FINAL BLANKING (Z) AMPLIFIER AND CRT

The blanking current derived from the Z pre-amplifier of the time-base unit is routed via common base amplifier V3200 and emitter-follower V3201 to the shunt-feedback amplifier V3202. This stage is fed by current source V3203, which gives a constant current of 4 mA. The voltage on the collector of V3202 can vary between +5 V for unblanking and -35 V for fully blanking.
This Z-pulse may contain d.c., l.f. and h.f. components to be applied to grid G1 of the CRT. Since G1 is at a cathode potential of -2000 V, blocking capacitors are required between G1 and the Z-amplifier output. The h.f. component is directly routed via blocking capacitor C3211 to G1.
However, the d.c. and l.f. components are blocked, so these components are first modulated on a 200 kHz carrier signal by V3207 and V3208 to pass blocking capacitor C3209. Then the signal is demodulated again by V3209 and V3211. Finally, the reconstituted d.c. and l.f. components are added to the h.f. component.

Transistor V3251 forms a nominal 70 V zener circuit which provides the voltage difference between the cathode and G1 of the CRT. This bias voltage ensures blanking when there is no input signal. For adaptation to each CRT, this voltage can be varied between about 40 V and 100 V by means of R3252 (BLACK LEVEL). Resistor R3254 keeps the filament at the same potential as the cathode.

Any ripple on the cathode voltage is fed-back via transistor V3213 to the input of the Final Z-amplifier and added to the blanking signal. This means that the differential voltage between G1 and the cathode of the CRT is always fixed. Because this differential voltage determines the intensity of the spot, as a result, the intensity is almost independent of the ripple.

The amplifier stage V3253, V3254 and V3256 provides amplification for the range of the FOCUS control. The range of 0...+10 V gives a final range on G3 of the CRT of -1350 V ... -1600 V.

Resistor R3257 connects the INTENS control to the focus adjustment to maintain a sharply defined trace at varying brightness.

For optimum presetting of the GEOMETRY, the voltage on G5 of the CRT is set to a fixed level of -30 V. The ASTIGMATISM can be varied by means of potentiometer R3267.

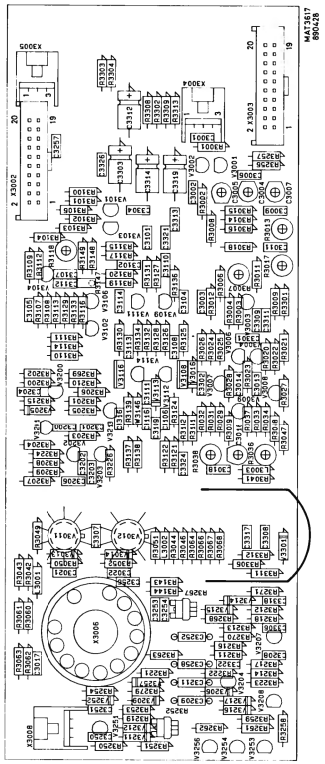
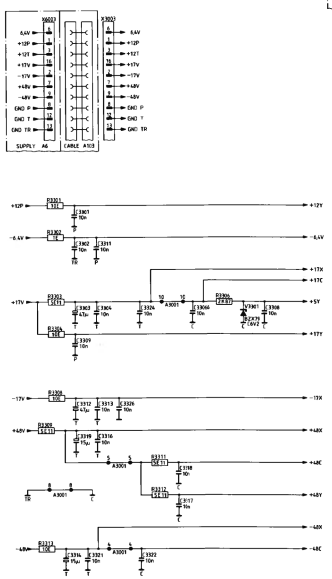


Figure 6.1 XYZ amplifier p.c.b.



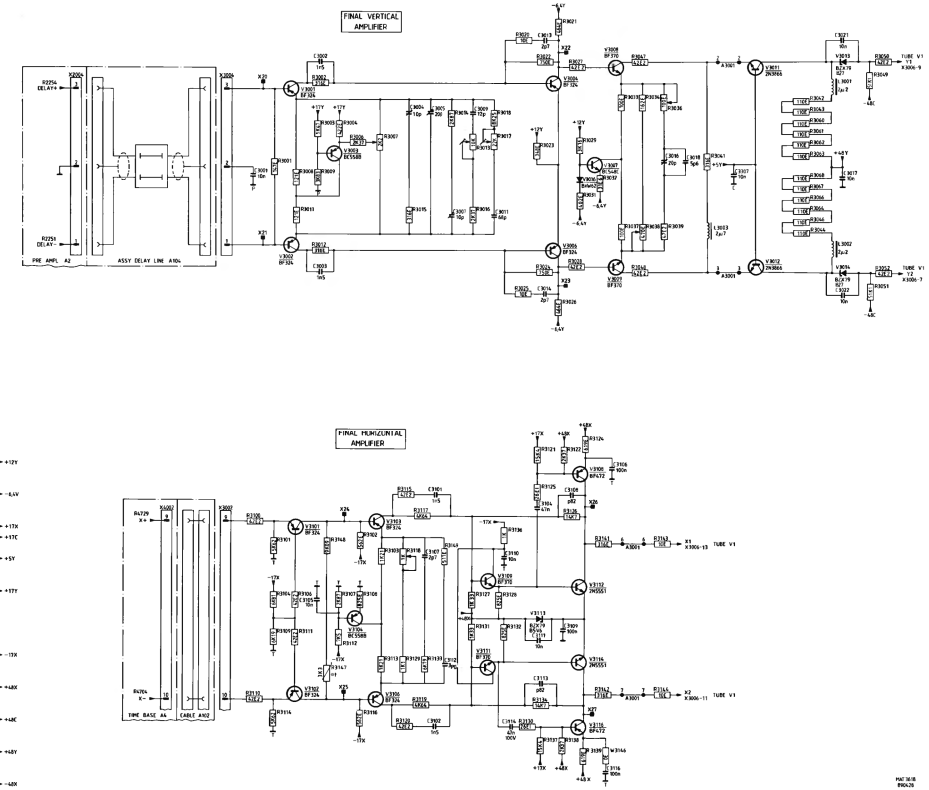


Figure 6.2 Circuit diagram of XYZ amplifiers, final X and Y amplifiers

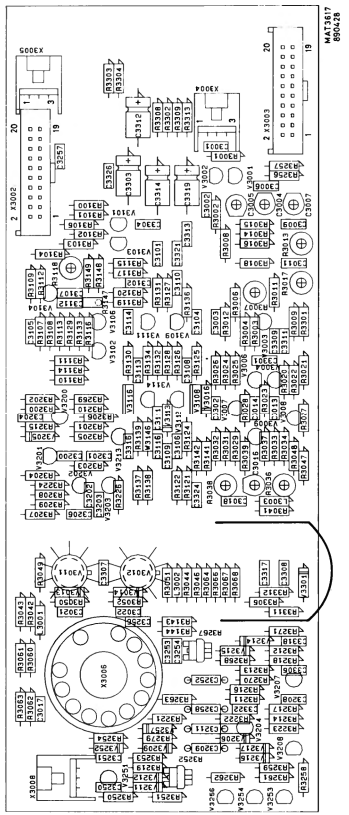


Figure 6.3 XYZ amplifier unit p.c.b.

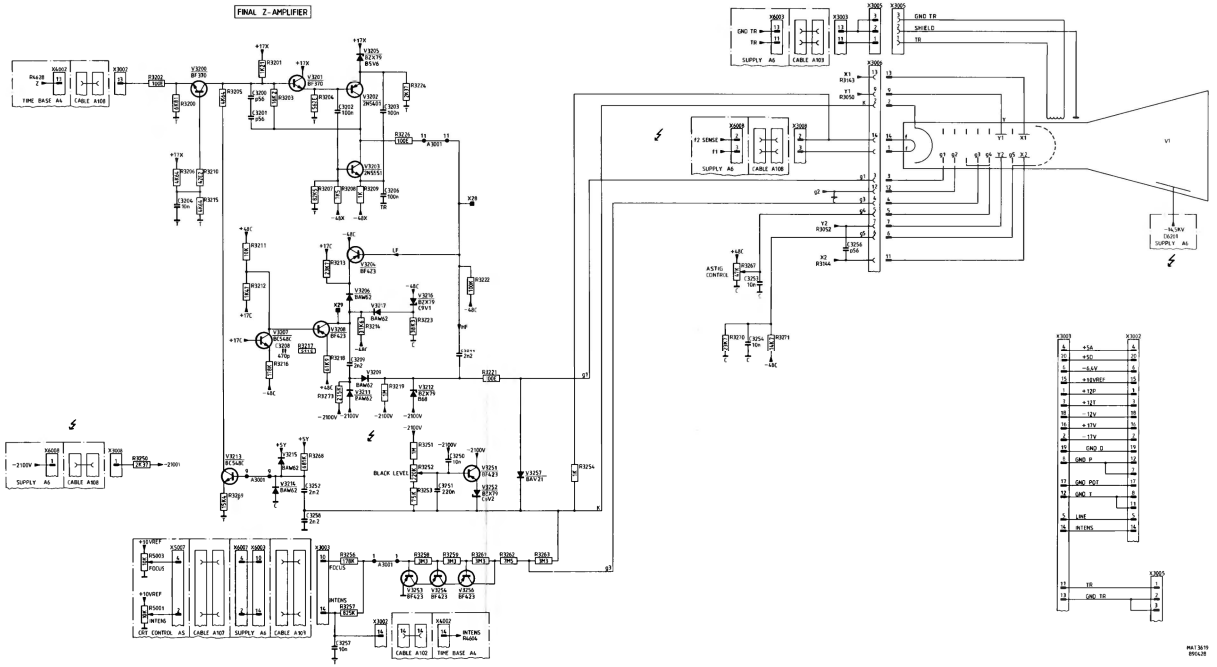


Figure 6.4 Circuit diagram of XYZ amplifiers, Z amplifier and CRT circuit

7. TIME-BASE UNIT (A4)

The time-base unit consists of:

- Trigger amplifier
- Timing circuit
- Sweep generator
- X DEFL amplifier, incl. display mode switch
- Horizontal pre-amplifier
- Z amplifier

As a supplement, the timing diagram for several conditions of the time base is given in section 7.7.

All control pulses for this unit are generated by the time-base control circuit, via the I^2C bus. Integrated circuits D4001 and D4002 convert this series DATA into the parallel control pulses, provided that DLEN TB1, and DLEN TB2 are HIGH.

7.1 TRIGGER AMPLIFIER

* TB triggering:

The symmetrical trigger current signals TRIGM+ and TRIGM- are derived from the pre-amplifier unit and converted into the asymmetrical trigger voltage via the summation amplifier V4004, the shunt feedback amplifier V4008 and the emitterfollower V4009. The summation amplifier adds the base signal voltage of V4004 (caused by TRIGM-) and the collector signal current of V4001 (caused by TRIGM+).

* TV triggering:

When the signal TVMTB goes LOW, the normal trigger path is blocked via V4022 and the trigger signal is routed via the TV trigger stage V4011...V4023. Transistor V4012 serves to clip the synchronisation pulse and LINE/FRAME selection is obtained by V4021. If the signal TVF/LINE is high, TV frames are detected by C4004 ... C4007. A low control signal serves line detection by C4007.

7.2 TIMING CIRCUIT (see figure 7.1)

The timing for the entire time-base circuit is obtained by D4103 together with its associated components.

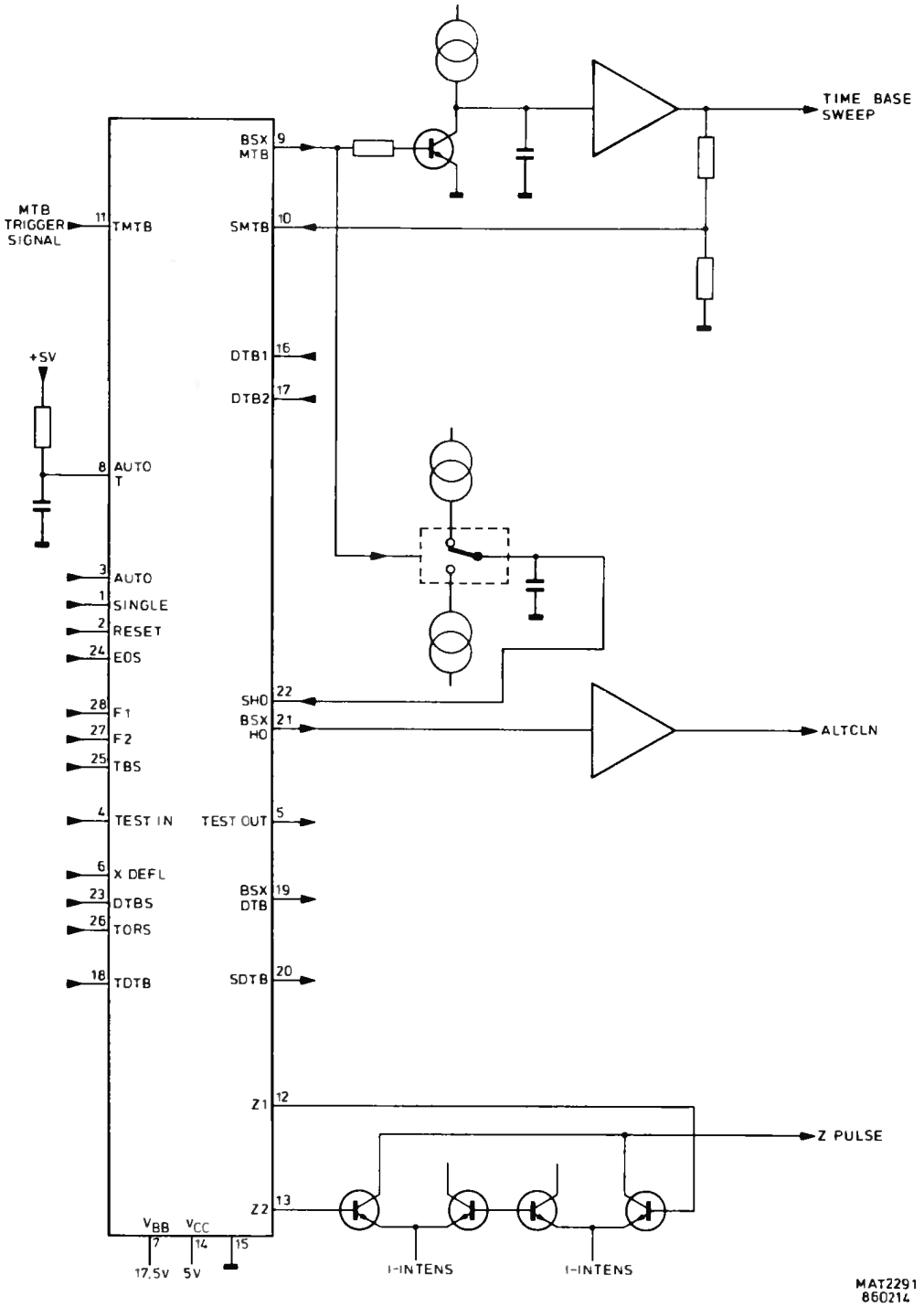


Figure 7.1 D4103 configuration

D4103 has the following relevant pin connections:

Pin	Name	INPUT-OUTPUT	Description
1	SINGLE	TTL-input	Selects the single time-base mode.
2	RESET	TTL-input	Stops the sweep and starts the hold off sweep.
3	AUTO	TTL-input	Selects the AUTO trigger mode, the time base is free-running after the last trigger pulse.
4	TESTIN	TTL-input	Selects the possibility to drive several functions (TESTOUT) in combination with SINGLE and RESET.
5	TESTOUT	TTL-output	--
6	X DEFL	TTL-input	Activates the Z1 and Z2 outputs.
7	Vbb	-	+1,5 V supply input.
8	AUTOTIME	input	RC-time determination (100 ms) for the AUTO trigger mode.
9	BSXMTB	TTL-output	Discharges the TB-sweep capacitor(s).
10	SMTB	SCHMITT-input	Determines the end of the TB-sweep.
11	TMTB	SCHMITT-input	Determines the start of the TB-sweep.
12	Z1	TTL-output	Determines the blanking of the CRT.
13	Z2	TTL-output	Determines the blanking of the CRT.
14	GND	-	Ground.
15	Vcc	-	+5 V supply input.
16	DTB1	-	not used
17	DTB2	-	not used, connected to ground.
18	TDTB	-	not used, connected to ground.
19	BSXDTB	-	not used
20	SDTB	-	not used, connected to ground.
21	BSXHO	TTL-output	Determines the ALT clock pulse
22	SHO	SCHMITT-input	Determines the end of the Hold-off sweep.
23	DTBS	-	not used; connected to supply +5Z.
24	EOS	-	Not used; connected to supply +5Z.
25	TBSX	TTL-input	Determines the TB-unblanking (HIGH)
26	TORS	TTL-input	Determines the STARTS condition (LOW) or TRIG'D condition (HIGH) of the DTB.
27	F1	TTL-input }	Determines the time base display
28	F2	TTL-input }	mode (both LOW).

NOTE: All SCHMITT-inputs are at +2,5 V level.

7.3 SWEEP GENERATOR

* TB sweep generator (see figure 7.2):

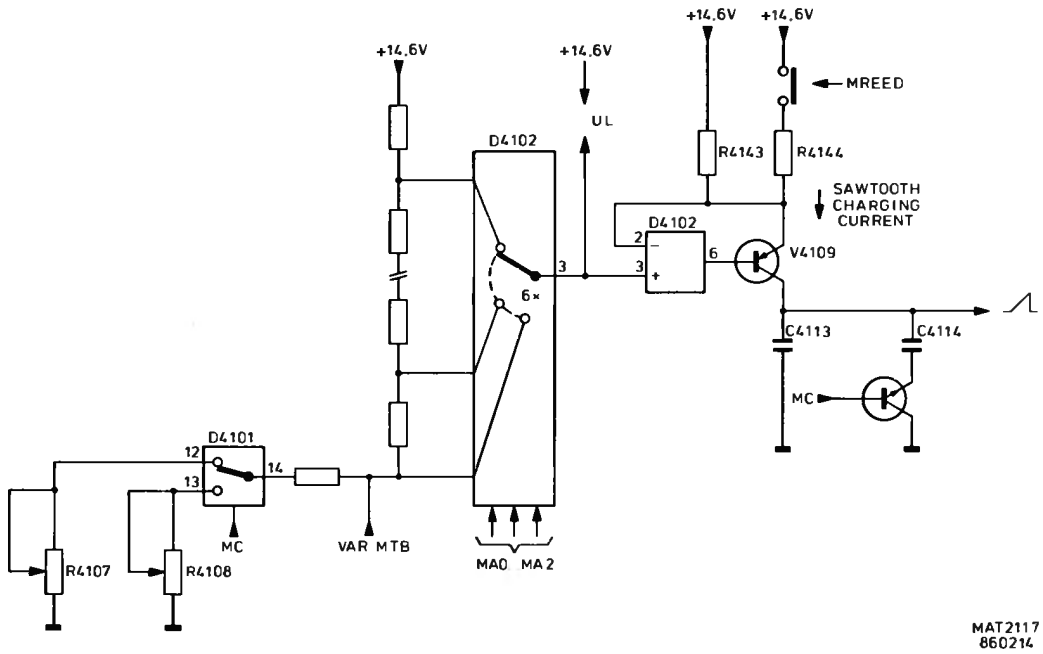


Figure 7.2 Simplified diagram of the time-base sweep generator

The sawtooth charging current $\frac{UL}{R4143 \text{ (and } R4144)}$ determines the sweep speed via C4113 (+C4114).
The circuit is controlled by the following address lines:

- MA0...MA2, for interconnection of D4102-3 to an input pin, thus giving six different voltage levels UL with respect to +14,6 V.
- MREED, for addition of R4144 to the sawtooth charging circuit.
- MC, for addition of C4114 to the sawtooth charging circuit and for switching over between calibration pot.meters R4107 (50ns...100us) and R4108 (200 us...0,5 s).

The voltage UL can be continuously varied by moving the VAR TB control R7009 from the CAL position. Thus a sweep variation of 1:2,5 can be obtained.

The function table for the sweep generator is given below:

sweep speed	MA2	MA1	MA0	MREED	MC
50 ns	1	1	1	0	0
.1 us	0	1	0	0	0
.2	0	0	1	0	0
.5	0	0	0	0	0
1	0	1	1	0	0
2	1	0	0	1	0
5	1	1	1	1	0
10	0	1	0	1	0
20	0	0	1	1	0
50	0	0	0	1	0
.1 ms	0	1	1	1	0
.2	1	0	0	0	1
.5	1	1	1	0	1
1	0	1	0	0	1
2	0	0	1	0	1
5	0	0	0	0	1
10	0	1	1	0	1
20	1	0	0	1	1
50	1	1	1	1	1
.1 s	0	1	0	1	1
.2	0	0	1	1	1
.5	0	0	0	1	1

NOTE: When MREED is low, then RELAY is switched on.

The sawtooth current is fed to the buffer circuit, where the h.f. sweep components (to 2 usec) are routed via C4116 and V4118, V4119.
The 1.f. sweep components (0,5 sec...2usec) is routed via N4103.

Finally the time-base sweep voltage is applied to the horizontal display mode switch.

* Hold-off circuit:

During the time base sweep, capacitor C4304 is discharged. In the lower sweepspeeds (lower then 10us) capacitor C4302 is also discharged via V4306. After the sweep, the capacitor(s) are charged via current source V4304 until the voltage across C4304 reaches the +2,5 V level. This voltage is applied to D4103 as the SHO signal and determines if the time base can generate a new sweep.

Depending on the HOLD OFF control potentiometer R7011 adjustment, a part of the charging current leaks away via V4301 and thus continuously variation of the charging time (i.e. hold-off time) is obtained. When BSXMTB goes LOW, the time base starts to run again and at the same time C4304 (and C4302) are discharged again via V4309.

7.4 X DEFL AMPLIFIER AND DISPLAY MODE SWITCH

* X DEFL amplifier:

The circuit for converting the symmetrical X DEFL+ and X DEFL- signals into the asymmetrical voltage, applied to the display mode switch is identical to the trigger input. However, this circuit can be switched-off by diodes V4500 and V4505, provided that the X DEFL signal is HIGH.

* Horizontal display mode switch:

The three deflection signals for real time base, digital time base or X deflection are switched to the horizontal pre-amplifier via diode switches. These switches are under control of the signals X DEFL and TBS. The output of the circuit is applied to R4701 on the horizontal pre-amplifier stage. The logic table is given below:

X DEFL	TBS	Output
1	*	X DEFL signal
0	0	Digital time base
0	1	Real time base

7.5 Z-AMPLIFIER

* Z-switch:

The Z-switch N4601 is configured as two differential amplifiers with a common current output to R4625. The stage is supplied by a constant current source via pin 3 and pin 9. The inputs Z1 and Z2 are derived from the timer stage D4103 and determine the unblanking of the CRT. For this oscilloscope Z1 and Z2 must be HIGH for normal intensity of the time base signal.
The amplitude of the Z-current can be varied by the front-panel INTENS control R5001. The slider of this control potentiometer drives the base pin 2 and pin 10 of both current sources.

To prevent burn-in of the CRT in the lower sweep speeds
0,5 sec...50 usec, signal ZB is LOW and reduces the voltage to pin 2 and pin 10.

Signal ZA is a software-controlled pulse to blank the trace when the AMPL/DIV switch is used.

* Z Pre-amplifier:

In normal condition, the full current for CRT blanking derived from N4601 is routed via R4625, V4612 and R2628 to the XYZ Amplifier A3.

However, there are two conditions for additional blanking:

- In the chopped mode of the vertical channels the display is blanked during switching over between channels. This happens by connecting the CHOPBLN pulse to V4611. When this pulse is HIGH, transistor V4611 conducts and a part of the blanking current flows via V4611 emitter-collector to the +5 K (+5V supply) rail.
- if a HIGH level is applied to the external Z MOD input on the rear panel, this signal causes conducting of V4616 so that a part of the blanking current flows via V4616 emitter-collector to the +5 K rail.

7.6 HORIZONTAL PREAMPLIFIER

The horizontal preamplifier drives the final X-amplifier on unit A6. It is a balanced amplifier that consists of V4702 and V4712. The amplifier receives the selected X-deflection signal. This signal can be the analog time base signal, the digital time base signal or the X-deflection signal. This signal is applied to the base of V4702. The base of V4712 receives a d.c. signal that determines the horizontal shift of the display on the CRT screen. The preamplifier can work with two different amplification factors:

- If X MAGN is inactive, the signal X10---LT is high. This has the result that V4706 is on and V4708 is off at the same time. The amplification is determined by the emitter resistors R4705 and R4718.
  V4707 serves as a constant current source.

- If X MAGN is active, the signal X10---LT is low. This has the result that V4706 is off and V4708 is on at the same time. The amplification is determined by the emitterresistors R4706, R4707, R4719 and R4721. This gives a 10 times gain increase compared with the other mode.

The signal that determines the horizontal shift of the signal is applied to the base of transistor V4712. This signal can be derived either from the X POS potentiometer via W4909 (during normal signal display) or via trimming potentiometer R4260 (during display of text and/or cursors). The selection is done in multiplexer D4101 under control of signal XPOSOFF-HT that is high during text display. The signal is low during display of the signal.

7.7 TIMING DIAGRAM

The following figure gives the timing diagram for D4103 for a free running time base sweep.

SINGLE	0
RESET	0
AUTO	1
TEST IN	0
X DEFL	0
TORS	0
F1	0
F2	0
DTBS	0
EOS	1
TBS	1

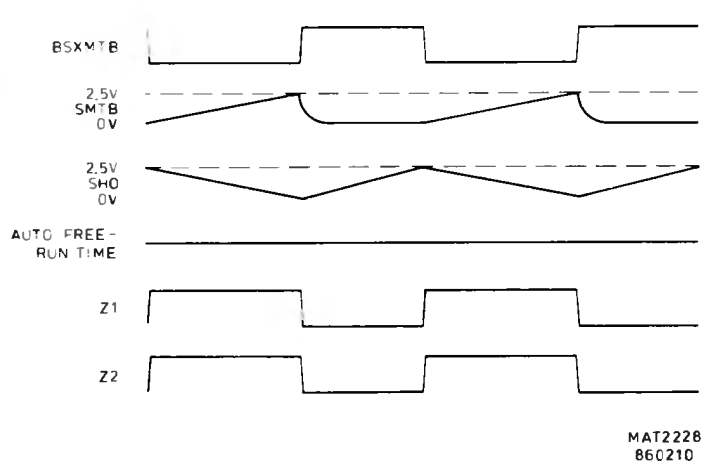


Figure 7.3 Free-running sweep-timing diagram

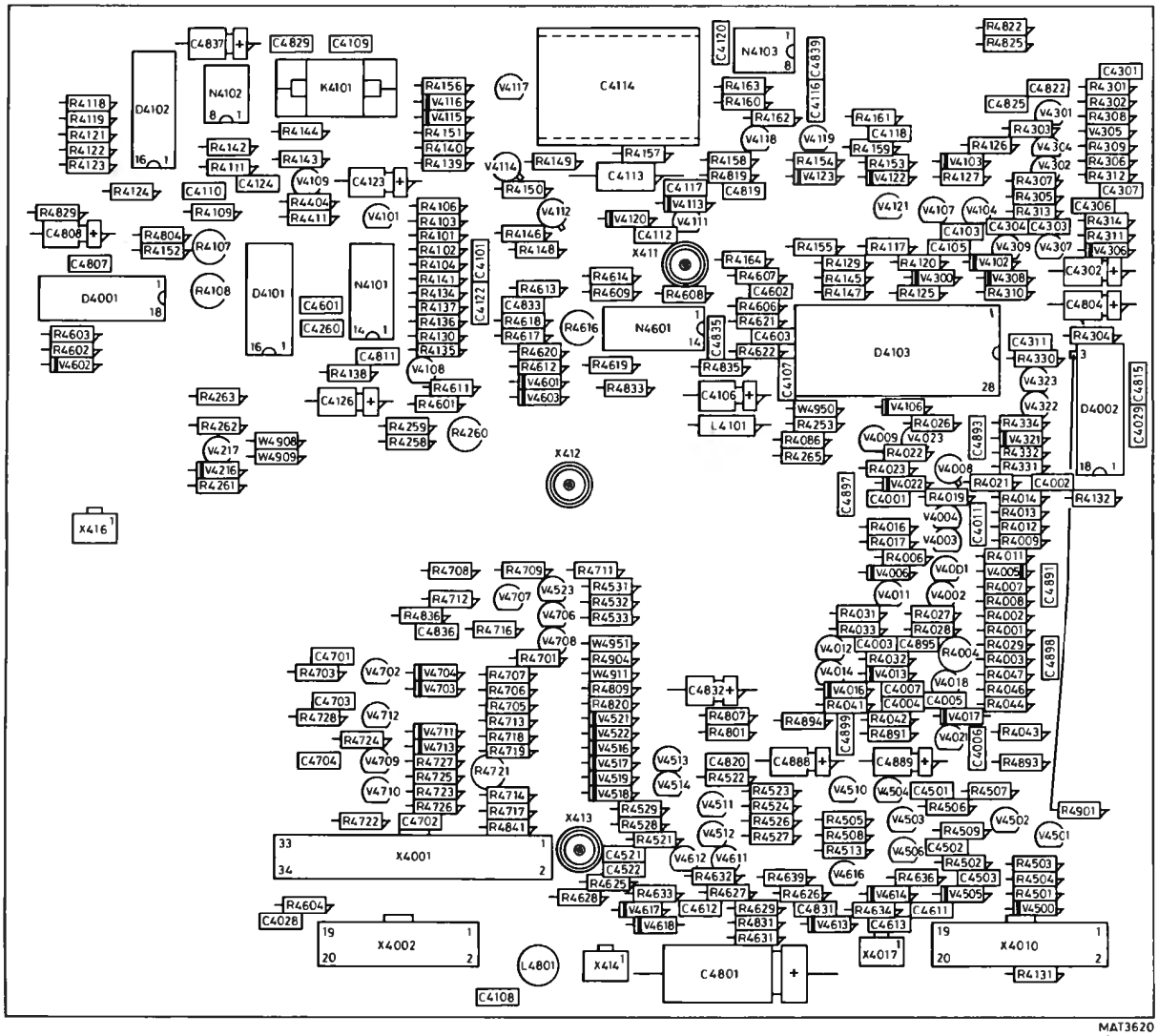


Figure 7.4 Time-base unit p.c.b.

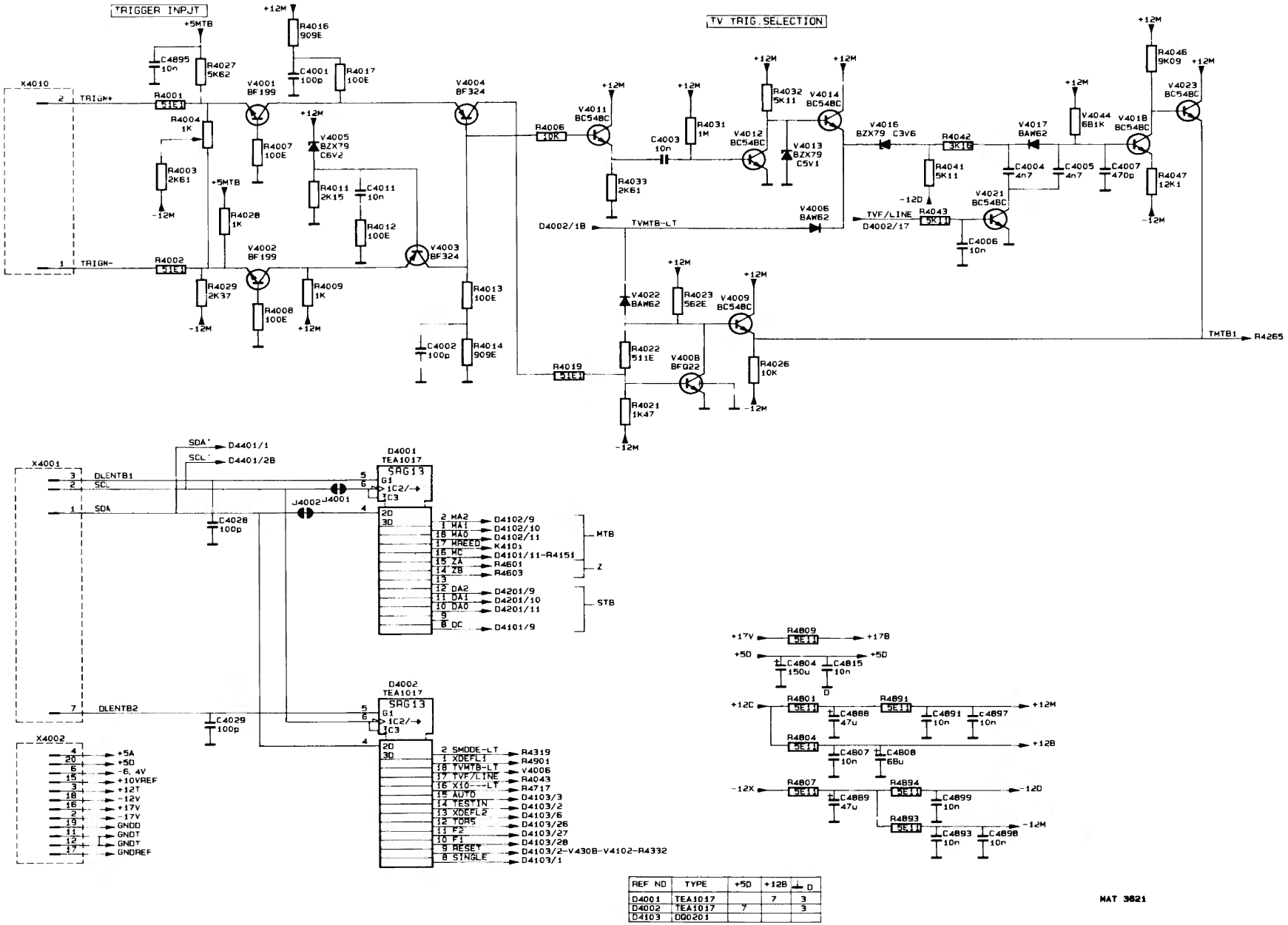
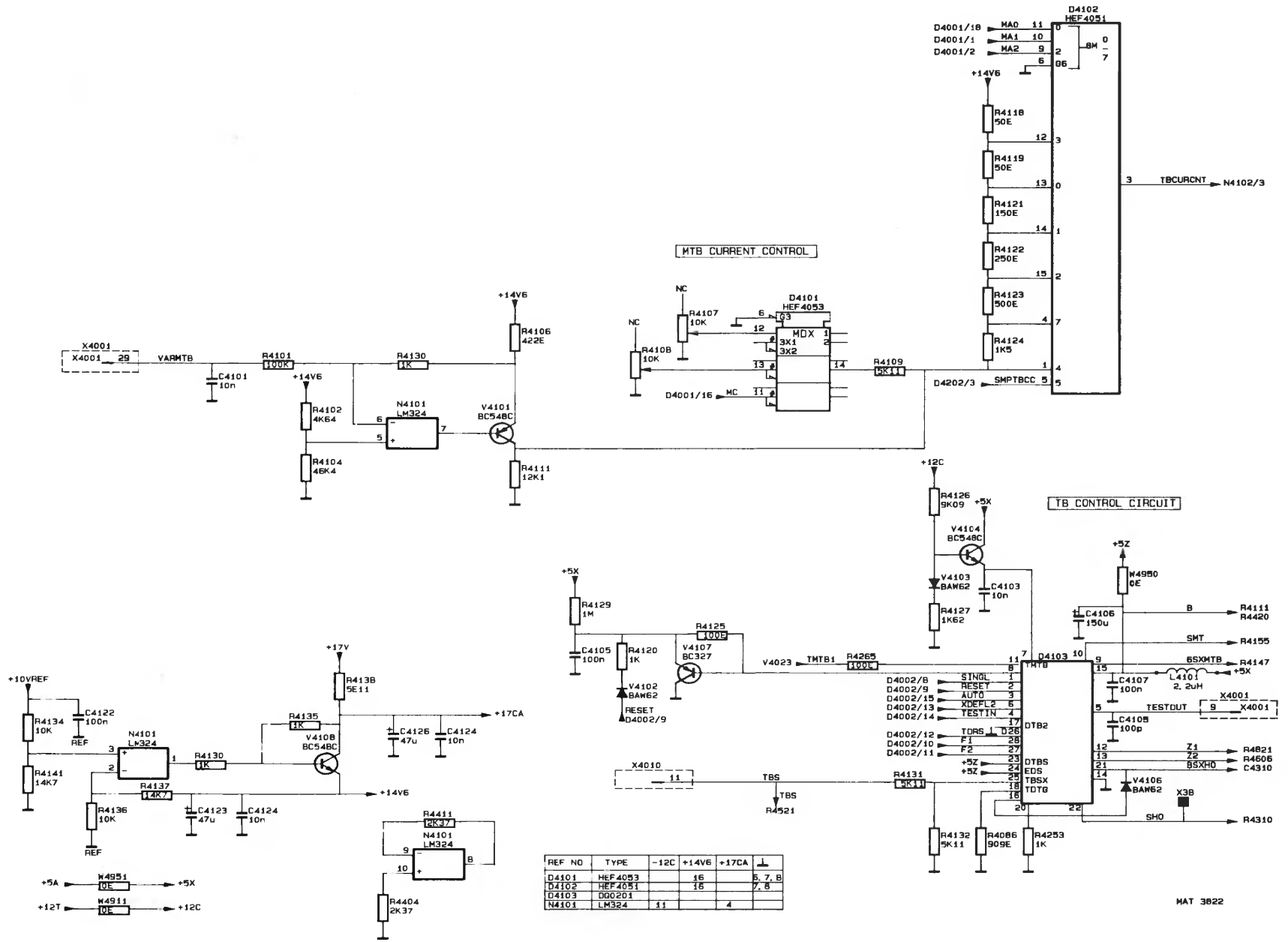


Figure 7.5 Circuit diagram of time-base, trigger amplifier



REF NO	TYPE	-12C	+14V6	+17CA	⊥
D4101	HEF4053		16		6, 7, 8
D4102	HEF4051		16		7, 8
D4103	DG0201				
N4101	LM324	11		4	

Figure 7.6 Circuit diagram of time-base, timing circuit and control

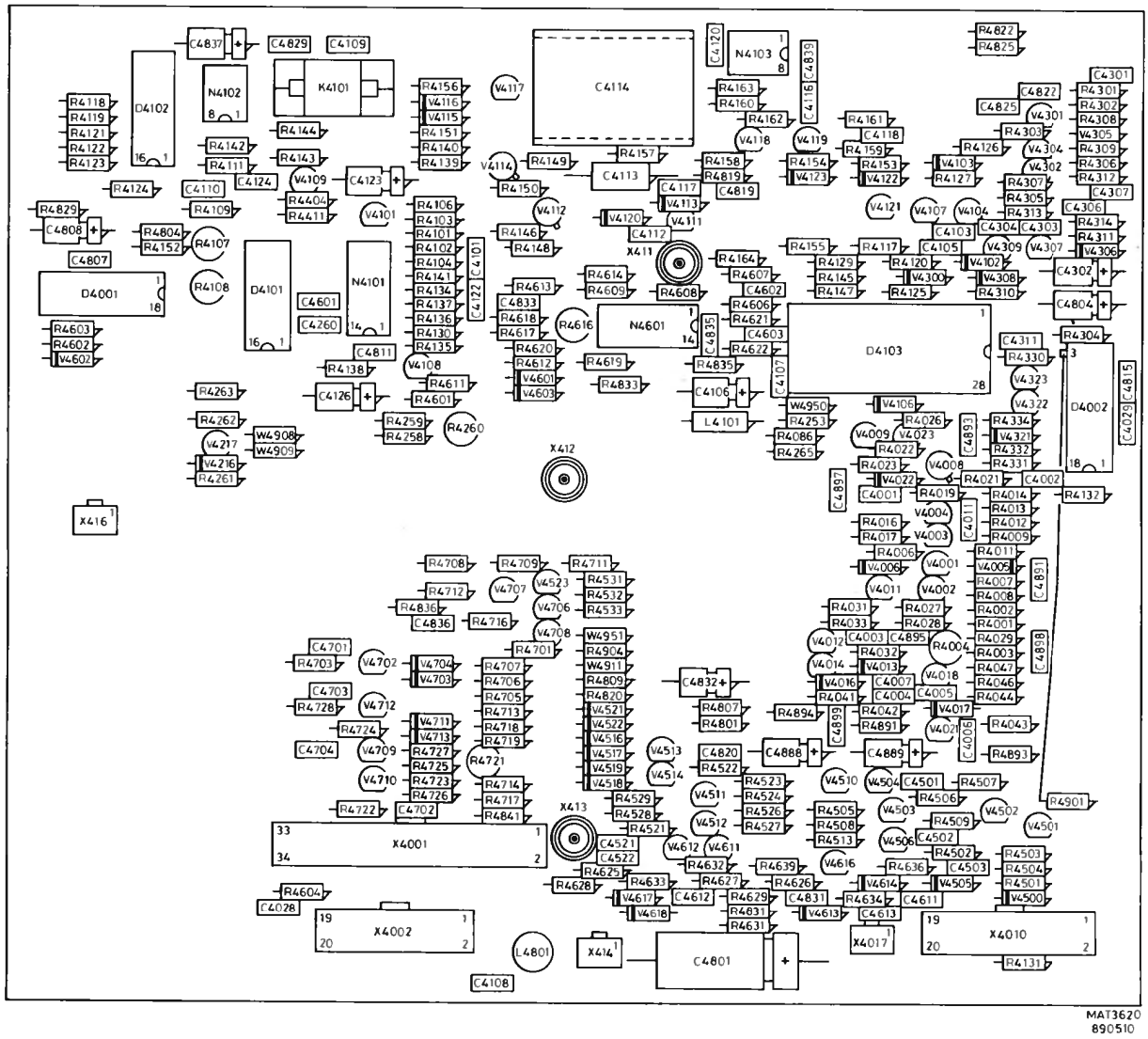


Figure 7.7 Time-base unit p.c.b.

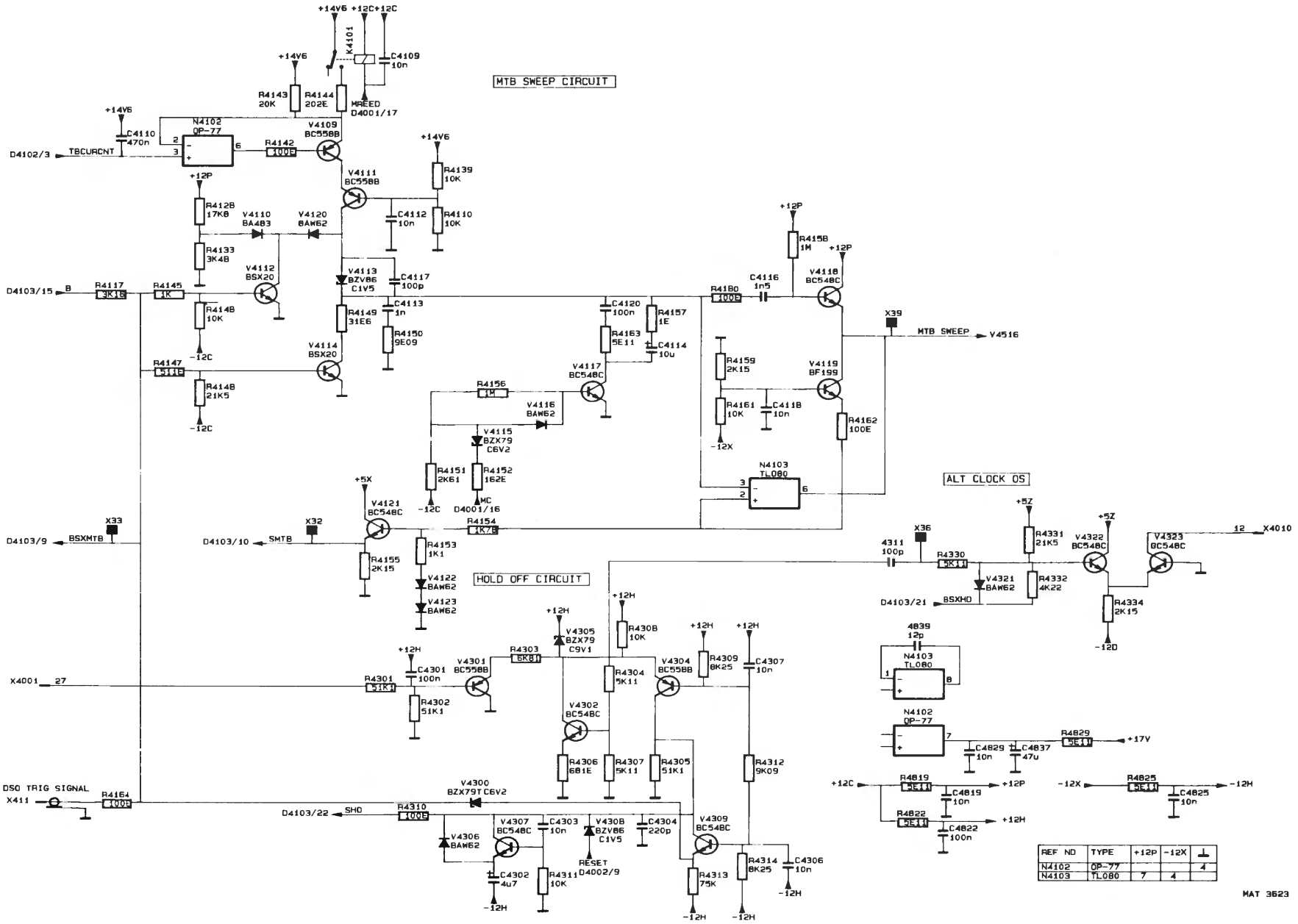


Figure 7.8 Circuit diagram of time-base, sweep generator and hold-off

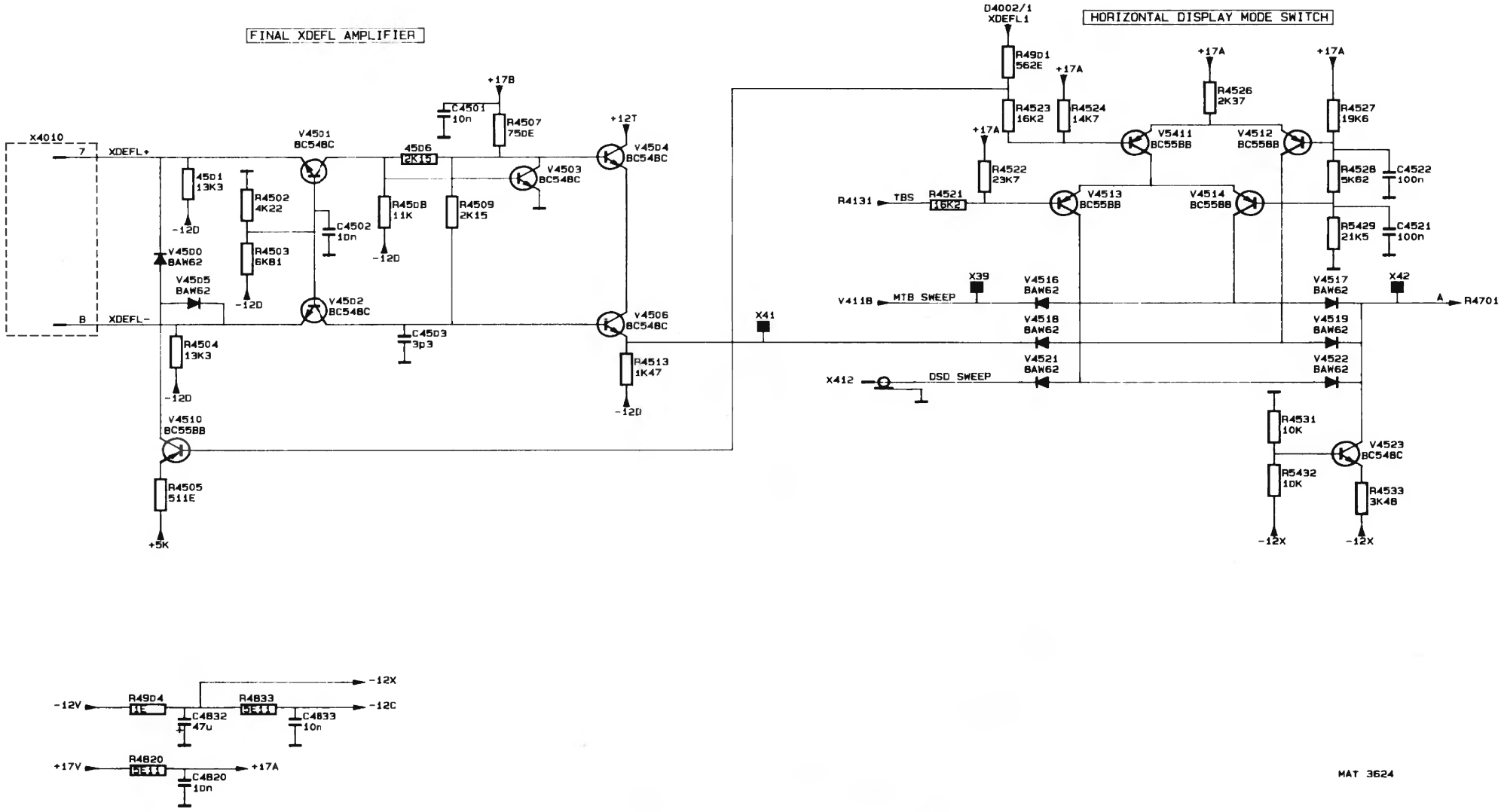


Figure 7.9 Circuit diagram of time-base, X-deflection selection

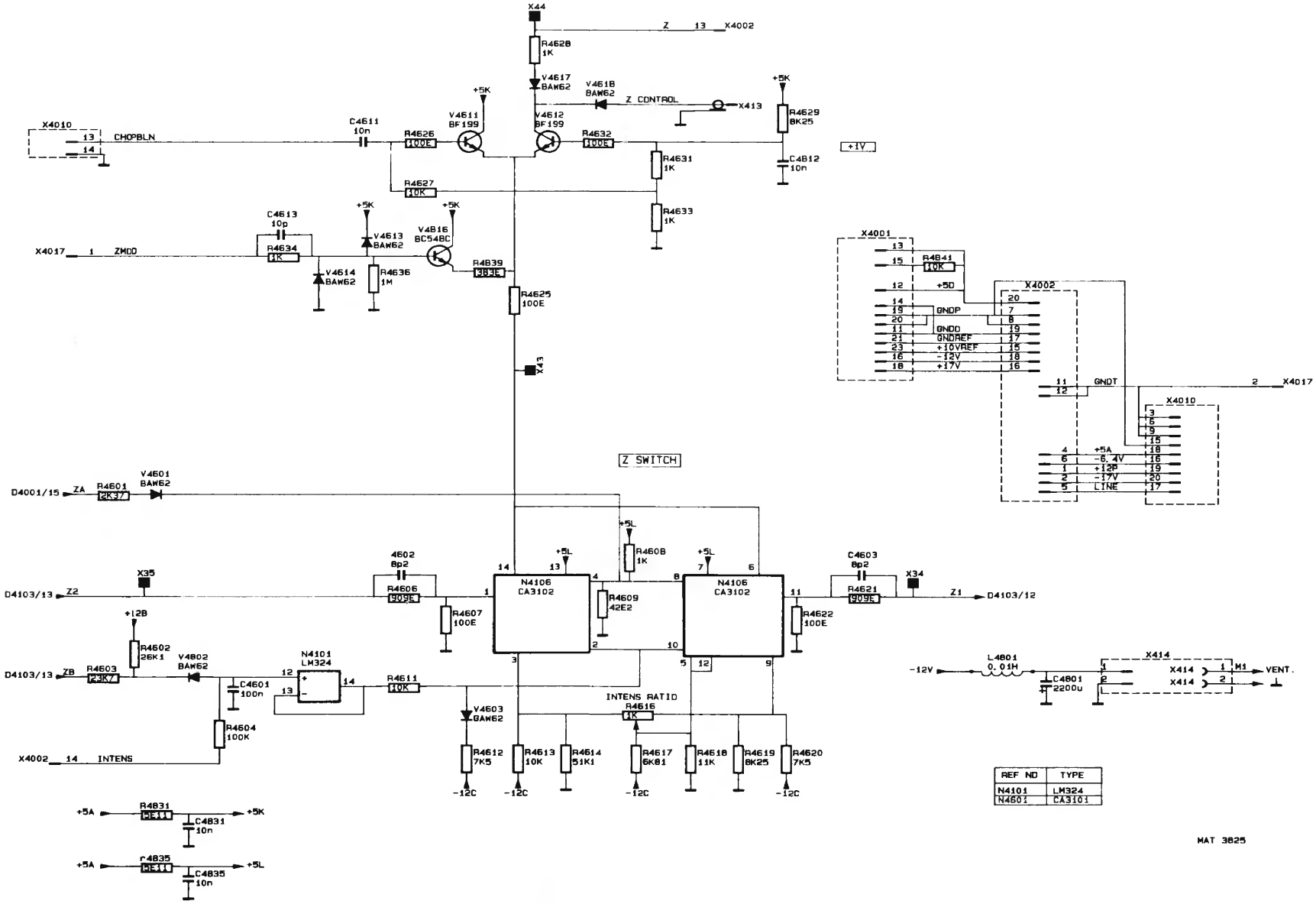


Figure 7.10 Circuit diagram of time-base, Z-amplifier

8. CRT CONTROL UNIT (A5)

This unit incorporates the potentiometers that control the CRT functions. These potentiometers are INTENS (R1), screwdriver operated control TRACE ROT (R2), FOCUS (R3) and ILLUM (R4).
The range of these potentiometers is between 0 V and +10 V.
The way these potentiometers influences the associated circuit is described together with the description of the relevant circuit part.

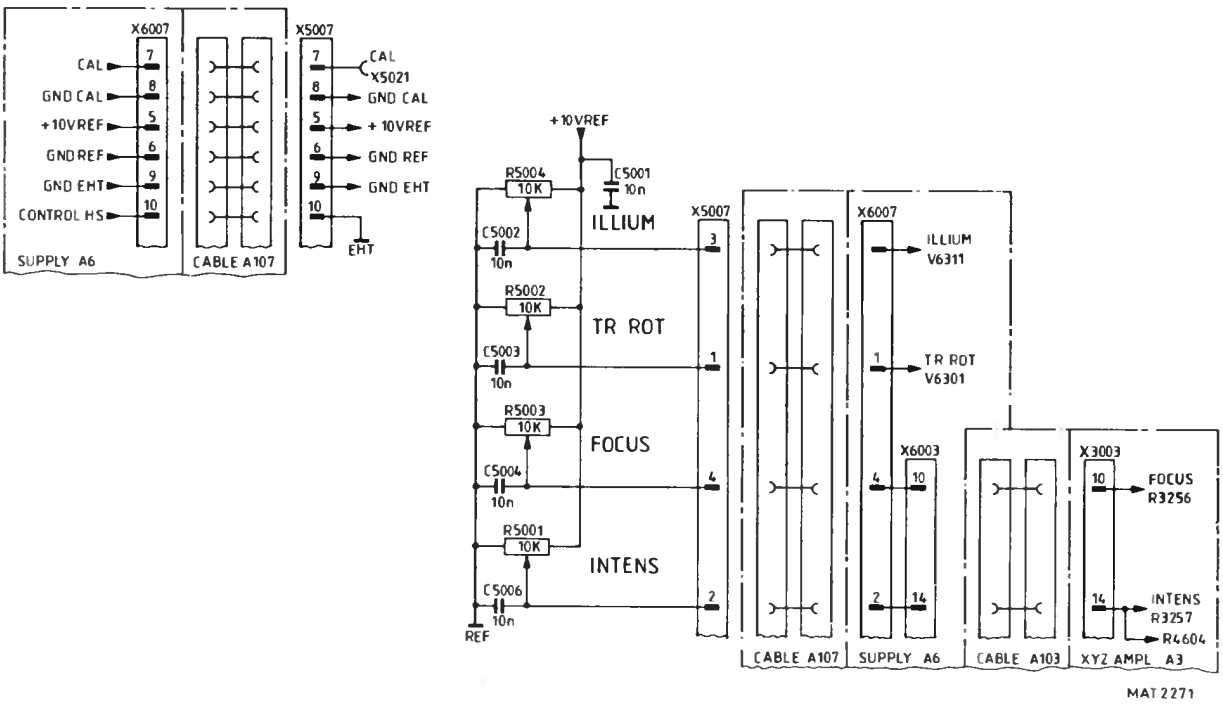


Figure 8.1 Circuit diagram of CRT control

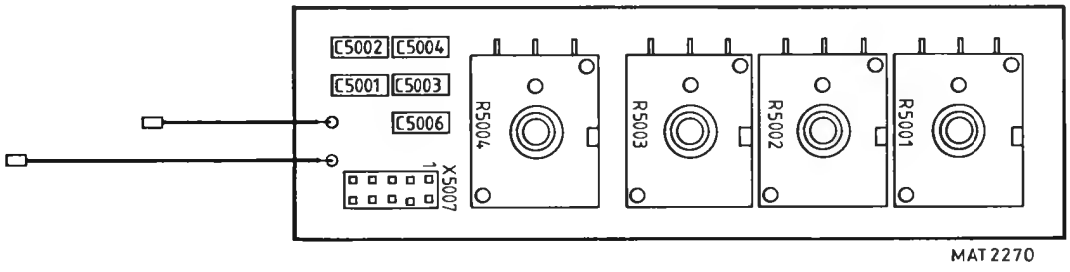


Figure 8.2 CRT control unit p.c.b.

9. POWER SUPPLY UNIT (A6)

Basically, the power supply unit consists of:

- input circuit
- converter circuit
- secondary output rectifiers
- HT supply
- CAL oscillator
- CRT control circuit

9.1 INPUT CIRCUIT

The instrument may be powered from a nominal mains voltage of 90 V...264 V a.c.
The mains voltage is primary protected by a fuse of 1 AT, which is located on the rear of the instrument.

After rectification by the diode bridge V6001...V6004 a d.c. voltage is applied to the converter circuit.
This voltage is smoothed by capacitors C6007, C6008 and three chokes.
Depending on the mains voltage, the rectified voltage is 120 V...370 V.

A fixed part of the mains voltage serves as a LINE-trigger signal.
The amplitude of the LINE trigger signal is 1/22x MAINS.

NOTE: The LINE trigger signal is <u>not</u> present when a d.c. voltage serves as MAINS.

9.2 CONVERTER CIRCUIT (see figure 9.1 and figure 9.2)

The flyback converters consists of transistor V6014 and V6018 and their associated components. The converter frequency depends on the LINE IN amplitude and is for 110 Vac: 30 kHz approx. For 220 Vac: 45 kHz approx.

Transistors V6014 and T6018 conduct on the forward stroke and charge transformer T6001. The thyristor V6013 fires when the voltage on the gate reaches the firing level (0,6 V approx). Consequently, V6018 blocks - V6014 blocks, for the duration of the flyback stroke, during which the secondary windings discharge via the diode rectifiers into the smoothing capacitors. The NTC resistor R6009 provides temperature compensation for the firing point of the thyristor.

During the flyback, capacitor C6009 charges again via the path T6001-1,V6012, V6009, R6004, C6009 and T6001-2.

The voltage stabilizer with transistor V6009 gives a square-wave to the gate of transistor V6014 with a maximum amplitude of 15 V.

The dv/dt limiter with L6004, L6006, V6017 and V6019 serves to eliminate the switching spikes present on the collector of V6018 (measuring point X46).

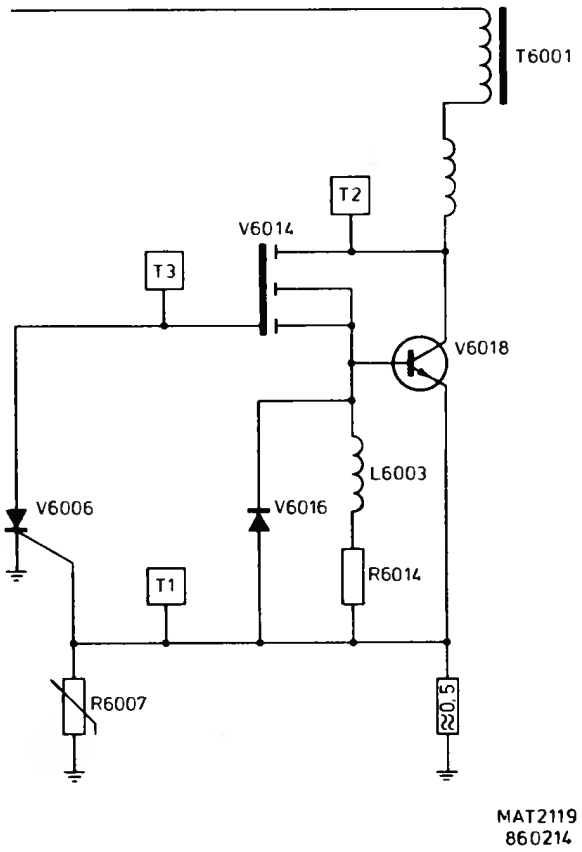


Figure 9.1 Converter circuit

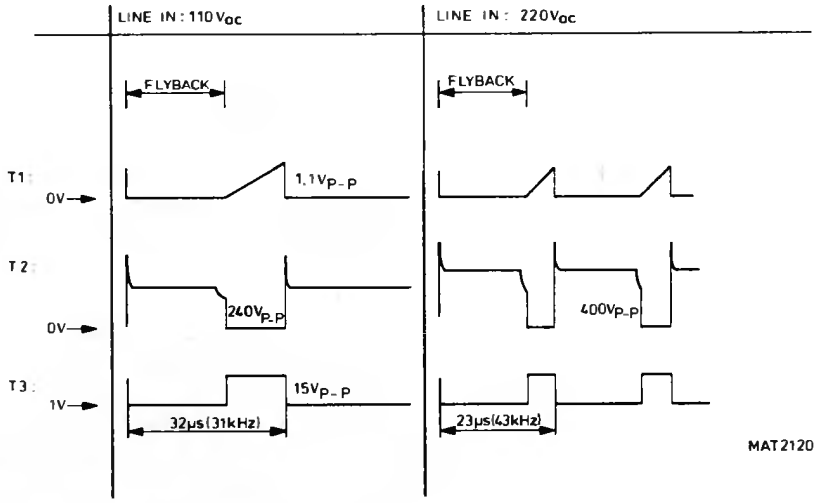


Figure 9.2 Timing diagram converter circuit

9.3 SECONDARY OUTPUT RECTIFIERS

The output voltages taken from the secondary windings of transformer T6001 are rectified by diodes and smoothed by capacitors in conventional circuits.
A "CROWBAR" circuit with transistor V6137 and V6112 protects the +5 V supply.
When the +5 V level is too high, transistor V6137 (and V6112) conduct and the power supply goes into short circuit mode.

A voltage protection circuit using V6134, V6136 and V6112 protects against overloads protection. When the power supply is overloaded, these components conduct and the power supply goes into in the short-circuit mode.

9.4 HT SUPPLY

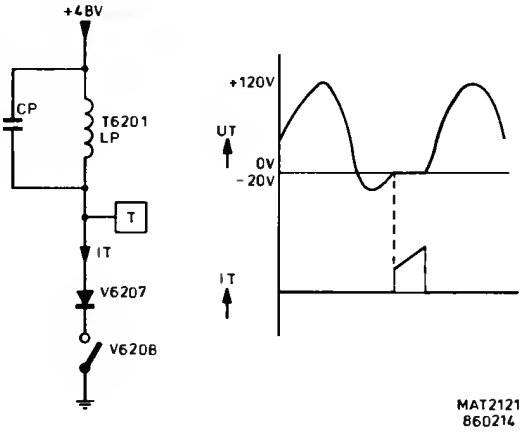


Figure 9.3 HT oscillator

The HT supply consists of an oscillator and a regulator circuit. Transformer T6201 determines the frequency (50 kHz approx.) of the oscillator. The output signal voltage on the secondary winding of T6201 is rectified by diode V6209 and smoothed by C6211. The -2,1 kV is also converted to +14,5 kV in the HT multiplier D6201 and routed via connector X6030 to the post-acceleration anode of the CRT.

To regulate this HT voltage the -2 kV is fed to the input of OP-AMP N6002.
The output level of N6002 determines the energy to T6201, and thus the amplitude of the HT-voltage.

9.5 CALIBRATOR

The calibrator circuit consists of two analogue switches D6501(8-9) and D6501(11-12) controlled by the active HIGH enable inputs 6 and 12 respectively, that are connected as an 2 kHz astable oscillator. Capacitor C6502 and resistor R6504 determine the 2 kHz frequency. The oscillator outputs, applied to enable inputs 5 and 13 of the second stage are in anti-phase with each other. Depending on the level of input 5 and 13, the CAL voltage will have a 1,2 V level or a 0 V level.

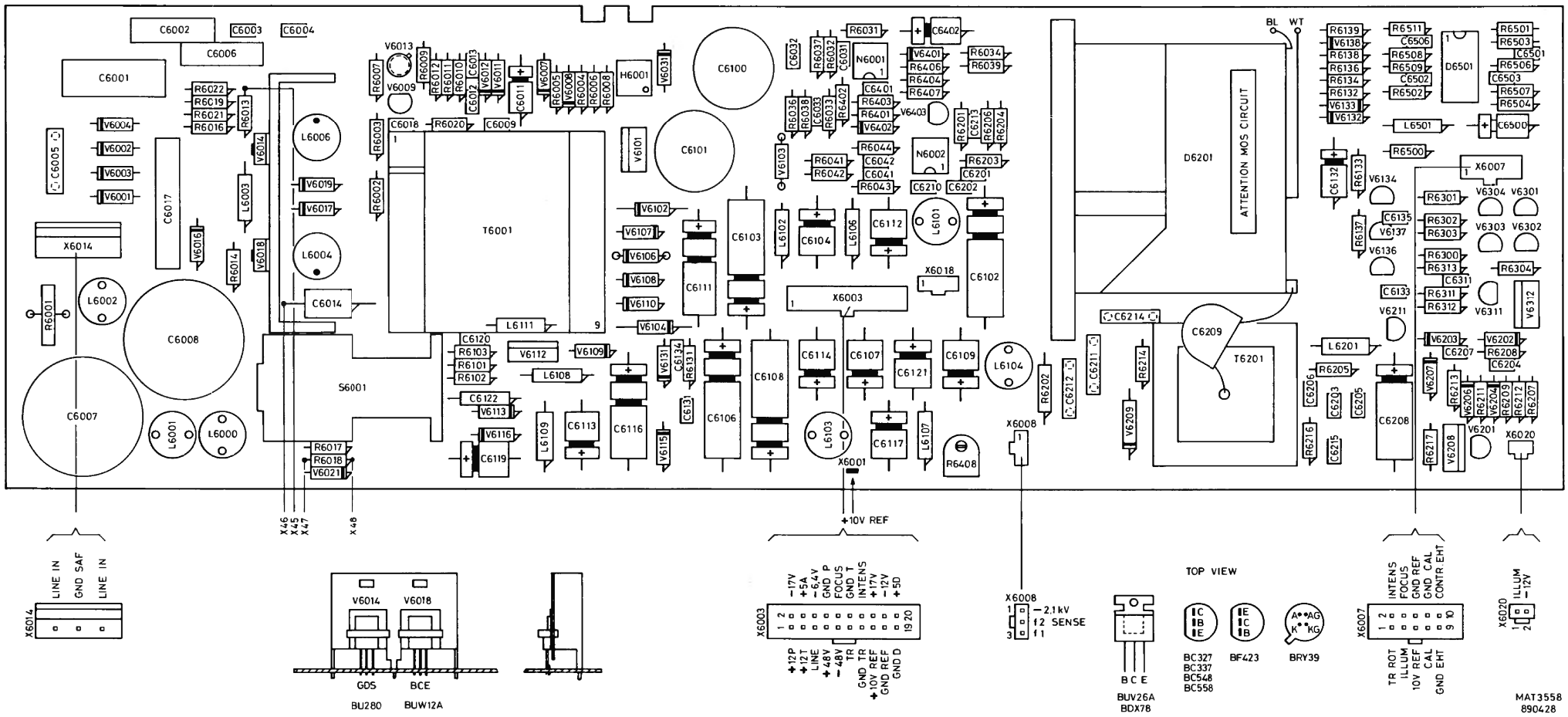


Figure 9.4 Power supply unit p.c.b.